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A Control Scheme for an AC-DC Single-Stage Buck-Boost PFC Converter with Improved Output Ripple Reduction

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A thesis submitted in partial fulfillment of the requirements for the degree in Master of Engineering Science

A Control Scheme for an AC-DC Single-Stage Buck-Boost PFC Converter with Improved Output Ripple Reduction

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ABSTRACT

AC-DC power factor correction (PFC) single-stage converters are attractive because of their cost and their simplicity. In these converters, both PFC and power conversion are done at the same time using a single converter that regulates the output. Since they have only a single controller, these converters operate with an intermediate transformer primary-side DC bus voltage that is unregulated and is dependent on the converters' operating conditions and component values. This means that the DC bus voltage can vary significantly as line and load conditions are changed. Such a variable DC bus voltage makes it difficult to optimally design the converter transformer as well as the DC bus capacitor.

One previously proposed single-stage AC-DC converter, the Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter has a clamping mechanism that can clamp the DC bus voltage to a pre-set limit. The clamping mechanism, however, superimposes a low frequency 120 Hz AC component on the output DC voltage so that some means must be taken to reduce this component. These means, however, make the converter transient slow and sluggish.

The main objective of this thesis is to minimize the 120 Hz output ripple component and to improve the dynamic response of the SSBBDET converter by using a new control scheme. In the thesis, the operation of the SSBBDET converter is reviewed and the proposed control method is introduced and explained in detail. Key design considerations for the design of the converter controller are discussed and the converter's ability to operate with fixed DC bus voltage, low output ripple and fast dynamic response is confirmed with experimental results obtained from a prototype converter.

Keywords: AC-DC power conversion, Power Factor Correction (PFC), Single-stage converter, Converter modeling

Dedication

With all my heart to my precious family and friends who gave me unconditional love and support throughout my entire life

Acknowledgments

I would like to thank my supervisor, Dr. Gerry Moschopoulos, for giving me the opportunity to join and collaborate with his research group during past two years. The accomplishments of this research would not have been achieved without his extensive support, encouragements and guidance.

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List of Acronyms and Abbreviations

AC	Alternating Current
BIBRED	Boost Integrated with Buck Rectifier/Energy storage/DC-DC
BIFRED	Boost Integrated with Flyback Rectifier/Energy storage/DC-DC
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
EMI	Electro-Magnetic Interference
IEC	International Electro-Technician Commission
IHQRR	Integrated High-Quality Rectifier-Regulator
PFC	Power Factor Correction
PWM	Pulse-Width Modulation
S^2IP^2	Single-Stage Isolated PFC Power
SSBBDET	Single-Stage Buck-Boost Direct Energy Transfer
THD	Total Harmonic Distortion

Chapter 1

Introduction

1.1. Power Electronics

Power electronics is a field in electrical engineering that deals with converting an available form of energy from a power source to the form required by a load. A power converter uses semiconductor devices such as diodes, MOSFETs and IGBTs to achieve this power conversion. Diodes are uncontrolled switches that turn on and conduct current when they are forward-biased and turn off when they are reverse-biased; MOSFETs and IGBTs are controlled switches that can be turned on or off by a switching signal at their gate (i.e. a high gating pulse is the turn-on command and a low or zero gating pulse is the turn-off command). A power converter can be an AC/DC converter, DC/DC converter, DC/AC inverter or AC/AC converter depending on the application. Many types of power sources can be used for these converters, such as AC single-phase, AC three-phase, DC source, battery, solar panel, or an electric generator. This thesis will focus on low power (< 100 W) single-phase, AC/DC converters.

Some sort of control method is needed to ensure that the output voltage of an AC/DC converter is regulated to the desired DC voltage. In a closed-loop power converter, a sensing circuit is responsible to send output voltage values (samples) to a controller circuit so that adjustments can be made to the power converter; typically this means changing the converter's duty-cycle. The term "duty-cycle" (D) refers to the proportion of on-time to the period T of the switch and is expressed in percent, with 100% as being fully on. It is by controlling the width of the on-time gating pulse relative to the switching cycle that allows the output voltage to be regulated. Such a

control method is generally referred to as Pulse-Width Modulation (PWM) in the power electronics literature.

1.2. Power Factor and Harmonic Distortion

The input power factor of an AC/DC power converter is an important consideration as it is a measure of how effectively the converter utilizes AC input power. Power factor is defined as the ratio of the real power flowing to the load to the apparent power in the circuit [1] and can be expressed as [2]

$$PF = \frac{real\ power\ (load\ power)}{apparent\ power} = \frac{\sum I_{sn,rms} V_{sn,rms} \cos\theta_n}{I_{s,rms} V_{s,rms}} \tag{1.1}$$

where $I_{sn,rms}$ and $V_{sn,rms}$ are rms values of the n^{th} harmonic of input current and input voltage, respectively and θ_n is the phase shift between them. Since the input AC voltage can be assumed to be a pure sinusoid, the product of voltage harmonic terms and current harmonic terms are zero with the exception of the product of fundamental voltage and current harmonics so that eq. (1.1) can be simplified to be

$$PF = \frac{I_{s1,rms}}{I_{s,rms}} \cos\theta_1 \tag{1.2}$$

where $I_{s1,rms}$ is the rms value of primary component of the input current. As can be seen from eq. (1.2), if the input current is a pure sine wave, then power factor can be defined as cosine of the phase angle between input voltage and current waveforms. Power factor can range from zero to one, with a power factor of one indicating that the input current is a purely sinusoidal waveform that is in phase with the input AC voltage.

Another term that is used for measuring the power quality of electrical power systems is Total Harmonic Distortion (THD). THD is defined as the ratio of the square root of the summation of the square of all non-fundamental harmonics of a waveform to fundamental component of the same waveform. For a current waveform, particularly the input current of a power electronic converter, it can be expressed as

$$THD_i = \frac{\sqrt{I_{2,rms}^2 + I_{3,rms}^2 + I_{4,rms}^2 + \cdots}}{I_{1,rms}} \tag{1.3}$$

where $I_{n,rms}$ is the rms value of the n^{th} harmonic of the input current.

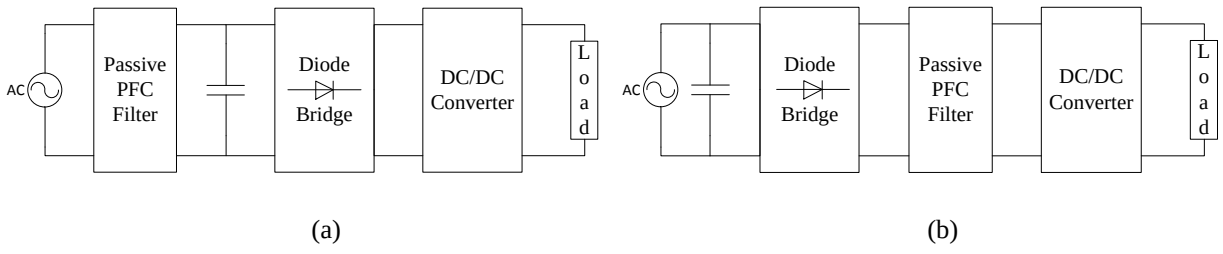
1.2.1. Standards, Regulations and Limitations for Harmonic Distortion in a Power Converter

The presence of non-fundamental input current harmonic components can have a negative impact on the operation of an AC/DC converter. This is especially true as they do not contribute to real power being delivered in the load, but they just circulate in the converter and create power losses, additional component stresses, heat and Electro-Magnetic Interference (EMI); they also limit the amount of power that can be delivered by the input AC source [2], [7].

The most negative effect that the input current harmonics of a power converter can have, however, is that they can corrupt the input AC source voltage. Since electrical equipment, household appliances, consumer electronics, lighting, computers, factory equipment, medical equipment, etc. – in short, anything that is powered from an AC utility source – has some sort of power electronic converter interface, and since all these generate input current harmonics that can be injected into the grid, the AC utility voltage would become distorted (which would negatively impact the operation of anything powered by it) were it not for the various standards that regulatory agencies have mandated to limit the input current harmonic content of power converters. One such regulatory agency is the International Electro-Technician Commission (IEC), which has produced current harmonic standards such as EN61000-3-2 that are commonly used to determine whether a particular electrical product can be sold in the marketplace [4]-[6].

1.3. Power Factor Correction (PFC)

With the exception of low power converters (< 75 W), most AC/DC converters in commercial products that are powered by the AC utility grid now have some sort of input Power Factor



(a) (b)

Fig. 1.1 Passive PFC with the filter on (a) the AC side, (b) the DC side of the diode bridge.

Correction (PFC). Input PFC techniques are needed to shape the input currents of AC/DC converters so that they have acceptable harmonic contents with their fundamental harmonic component in phase with the input AC voltage [9].

PFC techniques can either be passive or active. Passive techniques use passive elements such as inductors and capacitors in a low-pass or band-pass filter structure to filter low frequency harmonics [3]. These passive filters can either be placed at the converter's input AC side, as shown in Fig. 1.1(a) or in the intermediate DC link, as shown in Fig. 1.1(b) [10]. Although passive PFC techniques are simple and inexpensive, they have one significant disadvantage, which is their need for bulky capacitors and inductors. The size of these elements makes passive PFC techniques unsuitable for most applications except for low-power applications with narrow line voltage range.

1.3.1. Active Approaches for Power Factor Correction

Active PFC techniques are much more popular than passive PFC techniques. It is a generally accepted standard practice to implement a second active converter at the front-end of an AC/DC converter to perform input power factor correction as shown in Fig. 1.2. In other words, most AC/DC converters are two-stage converters than consist of an AC/DC front-end converter that performs PFC followed by a DC/DC converter that converts the output of the front-end converter into the desired output DC voltage.

The front-end AC/DC converter has a filter capacitor $C_{storage}$ to smooth its output voltage and make it DC so that it can be fed to the input of the DC/DC converter. AC/DC boost (step-up) converters are typically used as front-end converters because of their relative simplicity and their effectiveness in shaping input currents [8]. Flyback and forward converter topologies are

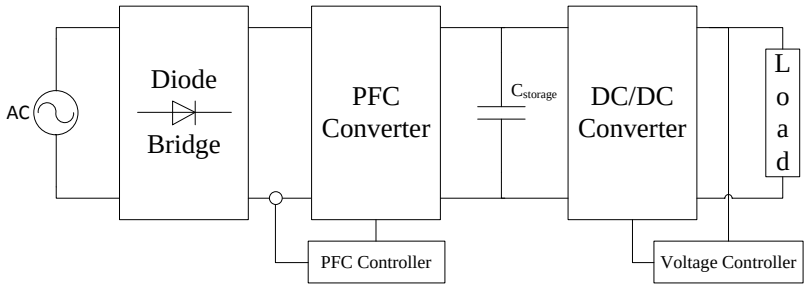


Fig. 1.2 Two-stage AC/DC PFC converter.

typically used as DC/DC converter in applications that are < 200 W, which is the focus of this thesis. The main drawback of two-stage converters is the cost and complexity that is associated with operating two separate and independent switch-mode power converters. As a result, power electronic researchers have been motivated to find alternative approaches to conventional two-stage AC/DC converters.

1.4. Single-Stage Active PFC Techniques

Single-stage PFC converters that combine PFC front-end converters and DC/DC converters into a single converter stage are a cheaper and less sophisticated alternative to conventional two-stage AC/DC converters [13]-[26]. They are operated with only a single controller to regulate the output DC voltage as they just have one converter stage, which for low-power applications (< 200 W) has just a single active semiconductor switch (typically a MOSFET). This is in contrast to conventional two-stage converters that have two controllers – one to regulate the output DC voltage and the other to regulate the intermediate DC bus voltage that is the input to the DC/DC converter.

Since single-stage converters do not have a controller to regulate the intermediate DC bus voltage, this voltage can vary considerably as it is dependent on the input line and output load conditions. Unless some means is used to limit this voltage, it can reach to levels of up to 1000V in converters that are operating under high input line and light load conditions. The excessive level and the variability of the DC bus voltage results in the need for components that can handle high peak voltage stresses and that can operate under a very wide range of operating conditions.

Single-stage PFC converters can be categorized into the following three distinct types:

1) Single-stage converters with variable switching frequency
2) Single-stage converters with voltage feedback techniques
3) Single-stage converters with direct energy transfer

Each of these types is explained briefly below.

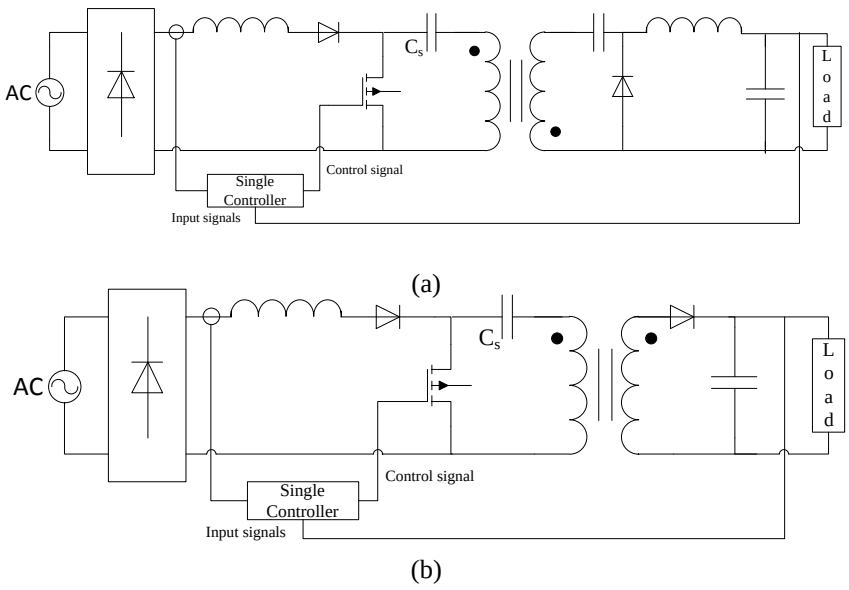


Fig. 1.3 Popular IHQRR single-stage PFC converters, (a) BIBRED, (b) BIFRED.

1.4.1. Single-Stage Converters with Variable Switching Frequency

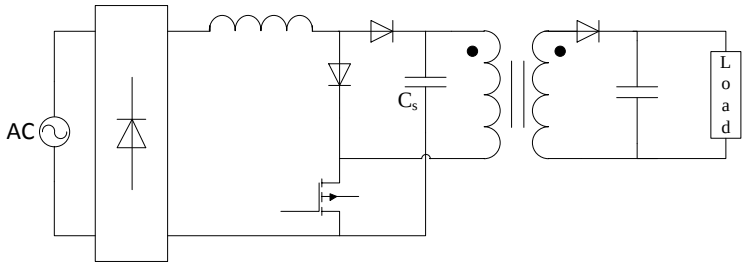
The Integrated High-Quality Rectifier-Regulator (IHQRR) [28] is one of the earliest types of single-stage AC/DC converters to be proposed. A DCM AC/DC boost converter (Discontinuous Conduction Mode, where the current of the input inductor reaches zero by the end of each switching cycle) and a DC/DC converter that operates in CCM (Continuous Conduction Mode, where the inductor does not discharge completely in any switching cycle) are combined in this topology. Fig. 1.3 shows an example of a BIFRED (Boost Integrated with Flyback Rectifier/Energy storage/DC-DC) converter and an example of a BIBRED (Boost Integrated with Buck Rectifier/Energy storage/DC-DC) converter, which are the most popular configurations of the IHQRR converter family.

Although the converters in this family operate with a nearly sinusoidal input current, their components suffer from high voltage stresses. To overcome this issue, the use of variable switching frequency control in BIFRED and BIBRED converters to reduce the voltage stress on the storage capacitor C_s was first proposed in [17]. The basic principle is that varying the converter switching frequency for varying load can affect the energy equilibrium that exists at the DC bus so that the DC bus voltage can be reduced. Operating with varying switching frequency can be complicated, however, and it is also difficult to design the converter components to operate over a very wide range of switching frequencies.

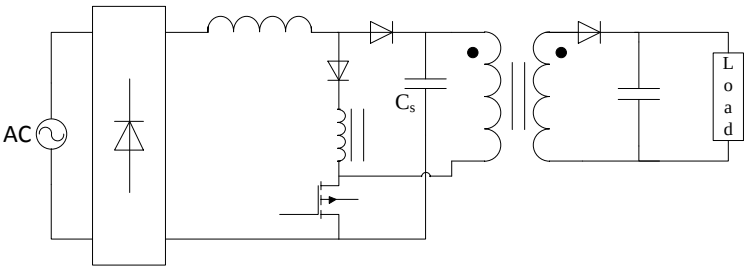
1.4.2. Single-Stage Converters with Voltage Feedback Techniques

To reduce the high voltage stresses on the semiconductor devices in IHQRR type single-stage converters so-called Single-Stage Isolated PFC Power (S^2IP^2) converters were proposed by R.Redl *et al.* [15, 16]. Fig. 1.4(a) shows the boost/single-switch flyback converter, the most popular topology of this family. The main characteristic of this family is that both the AC/DC PFC section and DC/DC section operate in DCM. Although S^2IP^2 converters have a lower DC bus voltage than IHQRR converters, this voltage can still be greater than 500V.

The DC bus voltage in S^2IP^2 and IHQRR converters can be reduced if some sort of DC bus voltage feedback technique is used, as shown in Fig. 1.4(b) [29-31]. In this technique, an auxiliary feedback winding that is coupled to the transformer is added to the converter. This winding acts as a negative feedback by preventing the full input voltage from appearing across the input inductor. Since less energy is stored in the input inductor when the converter switch is on, less energy is pumped into the DC bus capacitor when the switch is turned off. This affects the energy equilibrium of the DC bus capacitor so that the DC bus voltage is reduced; this voltage can be made to be less than 450V, which is considered to be a commonly accepted voltage due to the size of the DC bus capacitor. Although the DC bus voltage feedback technique



(a)



(b)

Fig. 1.4 (a) boost/single-switch flyback converter (b) DC bus voltage feedback in S^2IP^2 converters.

does decrease the DC bus voltage, it introduces distortion in the input AC current around its zero-crossing regions. This distortion is due to dead-band regions that must exist when the input voltage is low as no current can flow through the input diode bridge when the input voltage is less than the voltage across the auxiliary feedback winding.

A load current feedback technique in which an additional winding is added parallel to the transformer was later proposed in [32]. This technique is based on the same concept as the DC bus voltage feedback technique, but with a slight difference. This technique directly senses output power and adjusts input power at different loads, but in the DC bus voltage feedback technique, the input power is adjusted after DC bus voltage is increased because it feeds back output power indirectly using the DC bus capacitor voltage.

1.4.4. Single-Stage Converters with Direct Energy Transfer

In single-stage AC/DC converters with direct energy transfer, some of the power from the input source is processed only once in the converter, as shown in Fig. 1.5. As a result, these converters can operate with higher efficiency than other single-stage converters since some power from the input is processed only once instead of twice. A number of single-stage converters have been proposed [33-41] and Fig 1.6 shows a converter of this type that is based on a buck-boost input

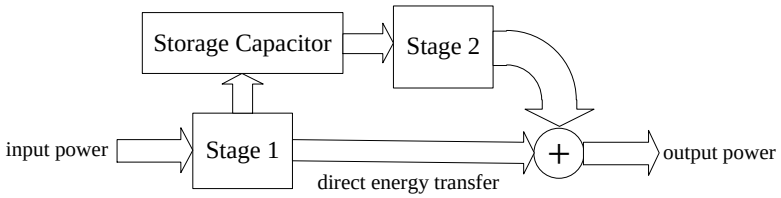


Fig. 1.5 Parallel PFC power processing diagram

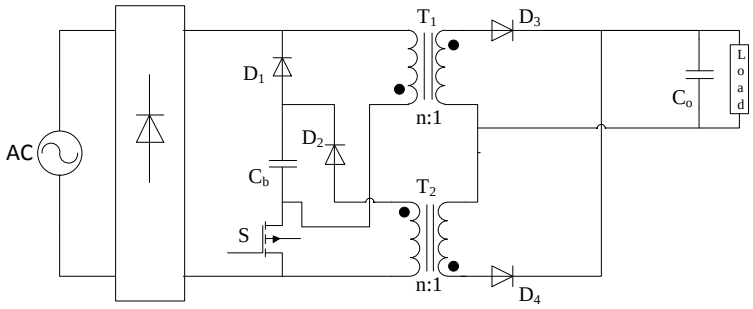


Fig. 1.6 Buck-boost single-stage PFC with direct energy transfer.

section that is proposed by N. Golbon *et al.* in [39]. The difference between the converter shown in Fig. 1.6 and a buck-boost single-stage converter without direct energy transfer is the addition of a second transformer to the circuit, T_1.

The main drawback of single-stage converters with direct energy power transfer is that their cost and complexity approach those of conventional two-stage AC/DC converters.

1.5. Control Approaches for Single-Stage PFC AC/DC Converters

The main challenge in operating single-stage PFC converters is the availability of only one control variable to achieve tight output voltage regulation and sinusoidal-like input current shape simultaneously. As a result, a tradeoff needs to be considered between output voltage regulation and input power factor in the design of the controller. Many control techniques have been designed for single-stage PFC converters [43]-[55]. They can generally be classifed as follows:

1) Peak current control
2) Hysteresis current control
3) Average current-mode control

Each of these control techniques is explained briefly below

1.5.1. Peak Current Mode Control

In peak current control, the positive slope of the input inductor current is controlled to be equal to a reference value in each switching cycle, regardless of other operating conditions. The switch

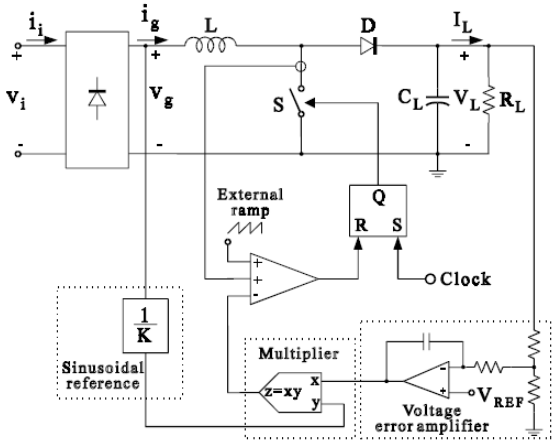


Fig. 1.7 Peak current control scheme on a boost PFC converter [42].

is turned off when the instantaneous current reaches the reference value. This limit point is defined based on the output voltage and input current status in each switching cycle. However, peak current control is inherently unstable when the duty ratio of the converter exceeds 50%. To stabilize the current feedback loop, a ramp signal (equal to the negative ramp of the input inductor current in a switching cycle) has to be added to the sensed current signal. This ramp should be calculated separately for each converter topology, based on circuit parameters and the output voltage.

Fig 1.7 shows peak current control implemented on a boost PFC front-end AC/DC converter (the same control scheme can be used for single-stage converters). The sinusoidal current reference is the product of the voltage compensator output and the sensed input voltage, and it is used to keep the input current in phase with the input voltage. This forces the voltage feedback loop compensator to have a low bandwidth so that 120 Hz low frequency ripple in the output voltage does not distort the input current reference waveform. In this scheme, the main switch is turned on with a constant frequency at the beginning of the switching cycle and is kept on until the sum of the sensed input current ramp and external ramp reaches the sinusoidal current reference.

The main advantages of this control scheme are that no current compensator is required for the controller and the switching frequency is constant. Peak current control, however, suffers from high sensitivity to noise because any noise spike in the input current can turn the switch off immediately. Furthermore, at high line and light load conditions where the control scheme is fully stable, the fixed compensating ramp signal can cause input current distortion.

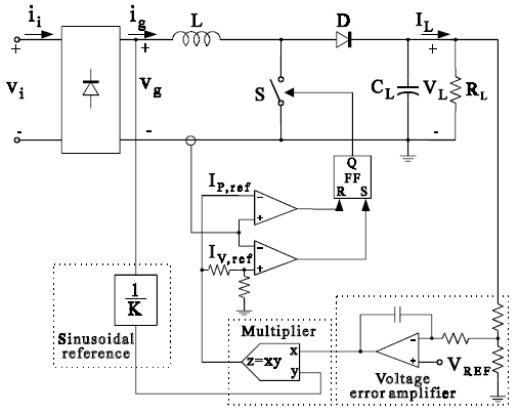


Fig. 1.8 Hysteresis current control on a boost PFC converter [42].

1.5.2. Hysteresis Current Control

This control method was first proposed in [57] and is based on restraining the input inductor current to be a preset hysteresis band. The switch is turned on when the inductor current goes below the predefined lower value and is turned off when the inductor current goes above the upper value; this forces the converter to operate with variable switching frequency [58].

Fig. 1.8 shows that two sinusoidal current references are required for this control technique - one for the peak of the input current and the other for its valley. To achieve smaller distortion in the input current, a smaller hysteresis band can be considered, but this leads to a higher switching frequency that increases switching losses [59]. The advantages of this control technique are an input current with little distortion and the lack of need of a compensation ramp; its main drawbacks are variable switching frequency operation and sensitivity to noise spikes.

There is a particular type of hysteresis control called "*borderline current control*" in which the switch on-time is kept constant during the line cycle [42] and the lower input current reference is set to zero. This allows the switch to be turned on when the input inductor current reaches zero and to be on until the input inductor reaches the upper reference value. With this control method, the converter operates at the boundary between CCM and DCM operation, instead of operating in CCM as in the original hysteresis control. Boundary mode operation results in lower switching losses because the switch is turned on at zero current. This control technique, however, has the same problems of variable switching frequency operation and sensitivity to noise spikes that the original hysteresis control technique has.

1.5.3. Average Current-Mode Control

The control methods reviewed in the previous sections all suffer from high sensitivity to commutation noise. The technique of "*average current-mode control*" in Fig. 1.9 addresses this issue by introducing a current compensator in the current feedback loop that allows a more sinusoidal input current in the converter. The inner current loop compensator in this control technique attempts to minimize the error between sensed input current and the current reference. This ensures a unity power factor and the reduction of higher order input current harmonics.

Since the input current tracks an average reference signal, the PFC converter operates in CCM with this control technique.

Like peak current control, the current reference in average current-mode control is the product of input voltage and the outer voltage loop compensator. As a result, the bandwidth of the voltage loop compensator should be very low (in 10-20 Hz range) to keep the output voltage ripple from distorting input current reference. The bandwidth of the input current loop compensator, however, should be very high (in 8-10 KHz range) to increase the accuracy of tracking higher order harmonics in the input current [60].

The main advantages of this control technique over previous approaches are more sinusoidal input current waveforms, fixed switching frequency and less sensitivity to noise, but it does require the design of additional compensation and it has a slow dynamic response because of low bandwidth of voltage feedback loop, like the other approaches. Nonetheless, average current mode control is generally considered as the best control approach for AC/DC PFC converters especially single-stage PFC converters.

1.6. Thesis Objectives

The main objectives of this thesis are as follows:

- To develop a mathematical model for the AC/DC single-stage PFC converter shown in

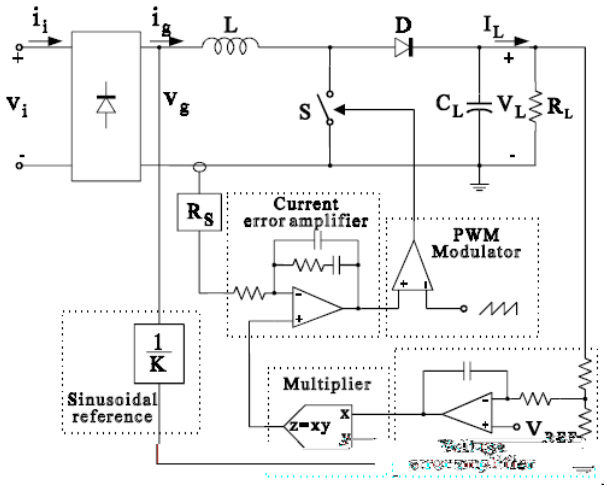


Fig. 1.9 Average current mode control on a boost PFC converter [42].

Fig. 1.6 so that an appropriate compensation network for the voltage and current feedback loops can be designed.

- To introduce a new control technique for this converter that will allow it to have a faster transient response, with tight output voltage regulation and with an input current harmonic content that is within the limits set by the IEC EN 61000-3-2 standard.
- To confirm the feasibility of the proposed control scheme with results obtained from computer and from an experimental prototype converter.

1.7. Thesis Outline

This thesis is comprised of five more chapters. Below is a summary of each chapter:

- **Chapter 2:** The single-stage AC/DC PFC converter with direct power transfer that was presented in Section 1.4.3 is the main focus of this chapter. This converter will henceforth be referred to as the Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter. In this chapter, the operation of the converter and its various modes of operation are explained in detail and key component values are selected by a design procedure. These component values were used in a prototype converter from which experimental results were obtained, as discussed in Chapters of this thesis.

- **Chapter 3:** A small-signal state-space model of the SSBBDET converter is determined in this chapter to be used for designing the voltage and current compensators of the proposed control scheme. In this chapter, the general approach for modeling PWM converters with one inductor operating in discontinuous conduction mode (DCM) is explained and is used to develop a new method of performing averaged state-space modeling for a PWM converter with multiple inductors operating in DCM, such as single-stage PFC converters. The main idea behind this new approach is that the averaged state-space model of a PWM converter with multiple inductors can be derived by first considering each inductor separately using the general averaged state-space model for PWM converters with one inductor, then adding all these separate models to obtain the model for the whole converter. It is shown how a small-signal model and key transfer functions can be extracted from the average state-space model of such a converter. The output to input small-signal transfer functions of the SSBBDET converter are used to

keep the small-signal values at zero so that the states of the system can operate at their pre-defined steady-state conditions.

- **Chapter 4:** A control strategy for the SSBBDET converter is proposed in this chapter. In this chapter, the conventional average current mode control approach that is generally used for single-stage PFC converters is discussed and its drawbacks are reviewed. A new control strategy based on conventional average current mode technique is introduced and a mathematical analysis of this technique is performed. The results of this analysis are used to select appropriate parameter values that ensure the proper operation of the SSBBDET converter with the new control scheme.

- **Chapter 5:** In this chapter, experimental results obtained from a prototype of the SSBBDET converter, implemented with the proposed control scheme described in Chapter 4 are presented. It is confirmed that the converter can operate with an excellent transient response and an acceptable input current harmonic content when implemented with the new control scheme.

- **Chapter 6:** In this chapter, the contents and results of the thesis work are summarized, the conclusions that have been reached as a result of this research work are presented, the main contributions of the thesis are expressed and possibilities for future research work are stated.

Chapter 2

A Low-Power AC-DC Single-Stage Converter with Reduced DC Bus Voltage Variation Using Direct Energy Transfer Technique

2.1. Introduction

The Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter that was presented in Section 1.4.3 of the previous chapter is the main focus of this chapter. The outstanding features of the converter are that it can operate with a sinusoidal input current and with a low primary-side DC bus voltage that is much less variable than that of other single-stage converters. In this chapter, the operation of the converter and its various modes of operation are explained in detail and key component values are selected by a design procedure. These component values were used in computer simulations and in a prototype converter that is discussed in the later chapters of this thesis. It should be noted that the contents of this chapter are taken from the work of N. Golbon and G. Moschopoulos in [39].

2.2. Converter Operating Principles and Modes of Operation

The SSBBDET converter (Fig. 2.1) consists of a diode bridge rectifier, a power switch S, transformers T_1 and T_2, a DC bus capacitor C, an output capacitor C_o, and rectifier diodes D_1 to D_4. T_1 and T_2 have turns ratios of n_1 and n_2 and magnetizing inductances of L_{m1} and L_{m2}, respectively. The leakage inductances of T_1 and T_2 are negligible.

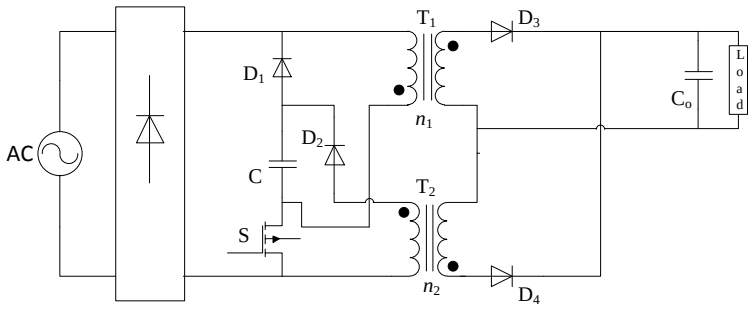


Fig. 2.1 Proposed buck-boost single-stage PFC with direct energy transfer.

The input current is discontinuous and is bounded by a sinusoidal envelope so that it is essentially a sinusoidal waveform with high frequency harmonic components. The magnetizing current of each transformer can be either discontinuous or continuous. To simplify the design, it is assumed that these currents are discontinuous so that both transformers are fully demagnetized by the end of the switching cycle.

The converter has two modes of operation, depending on the DC bus voltage V_C. In the first mode, transformer T_1 acts like an inductor (i.e. it stores an amount of energy during an interval and transfers this energy into another primary-side component on the next interval) while T_2 acts as a flyback transformer (i.e. it stores energy during an interval and transfers the stored energy to the secondary-side on the next interval). In the second mode, both transformers act like flyback transformers. Both modes are described in this section as following.

A. Mode 1: Single Flyback Transformer Mode of Operation

The converter operates in this mode when DC bus voltage V_C is less than n_1V_o, which is the reflected output voltage on the primary side of transformer T_1. As a result, diode D_3 does not conduct and no energy is transferred to the output through transformer T_1; therefore, T_1 becomes like an input inductor. In this mode, T_2 is the only transformer that actually operates as a flyback transformer. When operating in this single flyback transformer mode, the converter operates in the following two intervals. Typical converter waveforms and equivalent circuit diagrams are shown in Figs. 2.2 and 2.3:

Interval 1 [t_0 –t_1] (Fig. 2.3(a)): At the beginning of this interval, power switch *S* is turned on. As a result, the rectified input line voltage $|V_{in}|$ is applied to the magnetizing inductance of

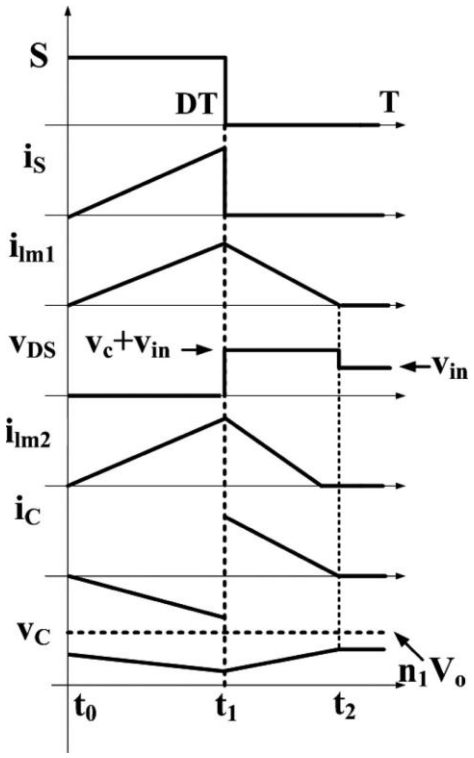


Fig. 2.2 Typical converter waveforms describing single flyback transformer mode.

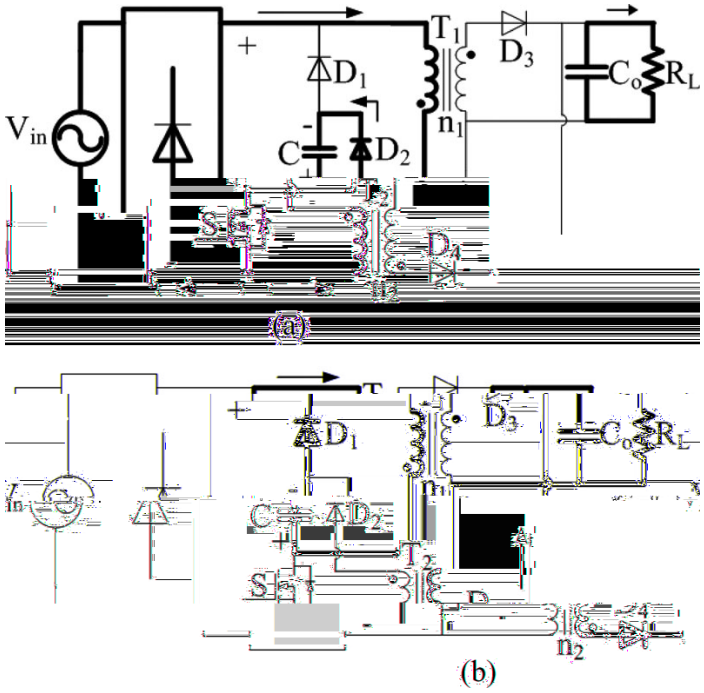


Fig. 2.3 Equivalent circuits in single flyback transformer mode (a) Interval I (b) Interval II.

transformer T_1, L_{m1}. Current through L_{m1}, i_{Lm1}, begins to flow and increase linearly. Also during this interval, DC bus voltage V_C is applied across the magnetizing inductance of T_2, L_{m2}, through D_2, causing its current i_{Lm2} to increase linearly. During this interval, there is no power transfer to the load and it is just supplied by C_o.

Interval 2 [t_1 –t_2] (Fig. 2.3(b)): Switch *S* is turned off at the beginning of this interval. As a result, all the energy that was placed in T_1 during Interval 1 is transferred to bus capacitor *C*, and all the energy that was placed in T_2 during Interval 1 is transferred to the output through D_4. At some instant $t = t_2$, both T_1 and T_2 become fully demagnetized and remain in this condition until the beginning of the next switching cycle.

B. Mode 2: Dual Flyback Transformer Mode of Operation

The converter enters this mode of operation when the DC bus voltage reaches n_1V_o. Ideally, V_C can never exceed n_1V_o because otherwise, diode D_3 starts to conduct and allow energy (which normally is supposed to charge the DC bus capacitor) to be transferred to the output. During this mode, both transformers T_1 and T_2 act like flyback transformers and demagnetize through their

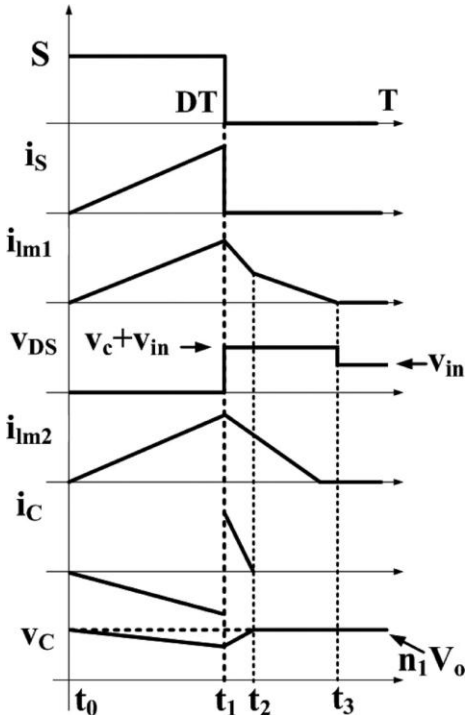


Fig. 2.4 Typical converter waveforms describing the dual flyback transformer mode.

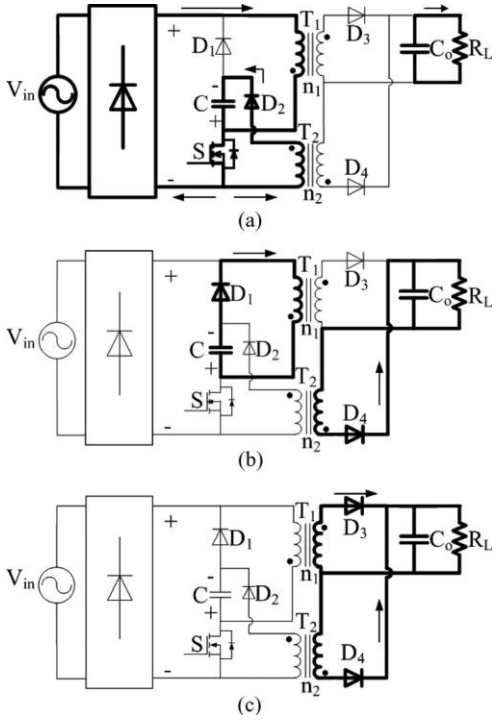


Fig. 2.5 Equivalent circuits in dual flyback transformer mode. (a) Interval I (b) Interval II (c) Interval III

secondaries when switch *S* is off. Part of the stored energy in the magnetizing inductance of T_1 goes to the DC bus capacitor after *S* has been turned off. When operating in the dual flyback transformer mode, the converter operates in the following three intervals with typical converter waveforms and equivalent circuit diagrams shown in Figs. 2.4 and 2.5, respectively.

Interval 1 [t_0– t_1] (Fig. 2.5(a)): The converter operates in the same way as the first interval of Mode 1 and transformers T_1 and T_2 are charged linearly.

Interval 2 [t_1 –t_2] (Fig. 2.5(b)): Switch *S* turns off at t_1 at the beginning of this interval. The converter operates in the same way as in the second interval of Mode 1 and the energy stored in T_1 is transferred to *C*. Also during this time interval, all the energy that was placed in T_2 in interval 1 is transferred to the output through D_4. The DC bus voltage reaches n_1V_o at $t = t_2$ while T_2 is not yet fully demagnetized.

Interval 3 [t_2 –t_3] (Fig. 2.5(c)): At $t = t_2$, V_C is equal to n_1V_o and D_3 begins to conduct as it becomes forward biased. This releases the remaining energy stored in T_1 to the output. Also

during this time interval, just as in interval 2, the rest of the energy that was placed in T_2 in interval 1 is transferred to the output through D_4. At different instants in this interval, T_1 and T_2 become fully demagnetized and remain in this condition until the start of the next switching cycle.

The advantages of the converter over conventional single-stage PFC converters are as follows:

1) The voltage stress on the main switch in this single-stage PFC converter is significantly lower than conventional ones. Regardless of operation mode, the maximum voltage that is placed across switch *S* occurs while T_2 is demagnetizing and is

$$V_{S,max} = n_1 V_o + V_{in} \tag{2.1}$$

2) There are two mechanisms that make the DC bus voltage less variable in this converter compared to previous single-stage PFC AC/DC converters. One is substitution of the input inductor with a flyback transformer, which helps clamp the DC bus voltage. The second is that the input section is based on a buck–boost converter instead of boost converter. In this case, the variation in the DC bus voltage can be reduced so that when the input line voltage is low, the buck-boost input section produces a DC bus voltage that is higher than the peak input voltage, and when the input line voltage is high, the DC bus voltage is lower than the peak of the input voltage. This is due to the nature of buck-boost topology (which can step-up and step-down voltage) as low input line operation requires larger duty-cycles, which makes the input section act as a boost converter. On the other hand, high line operation requires smaller duty-cycles, which makes the input section operate as a buck converter. The combination of these two mechanisms reduces potential voltage variation.

2.3. Steady-State Analysis and Converter Design

There are four key parameters that should be determined for the converter: the magnetizing inductances for transformers T_1 and T_2, L_{m1} and L_{m2}, and their turns ratios, n_1 and n_2. In this section, these four parameters are determined as well as the voltage conversion ratio of the converter (i.e. output DC voltage to input AC voltage). This can be achieved by performing a steady-state analysis of the converter then using the results of the analysis to develop a procedure that can be used to design the converter and select appropriate component values. Since such an

analysis has already been performed in [39], the analysis and design procedure is replicated from that work.

To simplify the analysis presented in [39], the following assumptions were made:

1) The converter is lossless.
2) The duty ratio of the converter is kept constant throughout the entire line cycle.
3) The switching frequency is much higher than the line frequency.
4) The leakage inductances of transformers are negligible.
5) Despite of slight changes in DC bus voltage, it is considered to be constant during each line cycle.

To derive the voltage conversion ratio of the converter, the balance between the input power and the output power should be considered. The converter peak input current $I_{in}(t)$ can be approximately expressed by the following equation, which is an equation of the voltage across the magnetizing inductance of transformer T_1, L_{m1}:

$$i_{in}(t) = V_m \frac{\sin(2\pi f_{line} t)}{L_{m1}} t \tag{2.2}$$

where V_m is the peak value of the input voltage, f_{line} is the line frequency, D is the duty ratio of the converter and T_{sw} is the switching time period. Since the switching frequency is much higher than the line frequency, the input voltage can be considered constant at each switching cycle. ($V_m \sin(\omega k)$ means the voltage in k^{th} switching cycle). As a result, the average input current in k^{th} switching cycle, $i_{in-avg}(k)$, can be derived as follows:

$$i_{in-avg}(k) = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_{in}(t)\, dt = V_m \frac{\sin(\omega k)}{2L_{m1}} D^2 T_s \tag{2.3}$$

The average power during k^{th} switching cycle can be determined to be

$$P_{avg} = V_m \sin(\omega k)\, i_{in-avg}(k) \tag{2.4}$$

and the average input power during half line cycle can be defined to be

$$P_{in-avg} = \frac{2}{T_l} \int_0^{\frac{T_l}{2}} P_{avg}(t)\, dt = \frac{D^2 V_m^2}{4 L_{m1} f_{sw}} \tag{2.5}$$

where T_l is the line time period and f_{sw} is the switching frequency.

With T_2 being fully demagnetized at the end of each line cycle, the average output power during a half line cycle can be determined based on the voltage across its magnetizing inductance. Since the DC bus voltage is constant during each line cycle, the following equations can be derived:

$$i(t) = \frac{V_c}{L_{m2}} t \tag{2.6}$$

$$i_{avg} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i(t)\, dt = \frac{V_c T_{sw} D^2}{2L_{m2}} \tag{2.7}$$

$$P_{out} = V_c i_{avg} = \frac{V_c^2 D^2}{2L_{m2} f_{sw}} \tag{2.8}$$

Considering the power balance in the circuit (i.e. $P_{out} = P_{in-avg}$), the following relation between the DC bus voltage, V_c, and the peak input voltage, V_m can be obtained based on (2.5) and (2.8):

$$\frac{V_m}{\sqrt{2}} = V_c \frac{\sqrt{L_{m1}}}{\sqrt{L_{m2}}} \tag{2.9}$$

The standard voltage transfer ratio equation of a flyback converter (if assuming that T_2 is working in boundary level of being fully demagnetized and not) can be applied to find the relationship between the DC bus voltage and output voltage as follows:

$$\frac{V_o}{V_C} = \frac{D}{n_2(1-D)} \tag{2.10}$$

where n_2 is the turns ratio of the transformer T_2. Using equations (2.9) and (2.10), the desired voltage conversion ratio of the converter can be determined to be

$$\frac{V_o}{V_m} = \frac{D\sqrt{L_{m2}}}{n_2(1-D)\sqrt{2L_{m1}}} \tag{2.11}$$

To find the key converter parameters (L_{m1}, L_{m2}, n_1, n_2), the following considerations should be taken into account:

1) The converter should operate with a completely discontinuous input current bounded by a sinusoidal envelope.
2) The maximum duty ratio during each line cycle should not exceed 0.5.

The above parameters will be designed for a converter with the following characteristics:

Input voltage: V_{in} = 85~265 V_{rms}

Output voltage: V_o = 48 V_{dc}

Maximum output power: P_o = 100 W

Switching frequency: f_{sw} = 100 kHz

A: Selection of magnetizing inductance of transformer T_1, L_{m1}

L_{m1} should be sufficiently low so that the magnetizing current of T_1 does not become continuous, which leads to Discontinuous Conduction Mode (DCM) operation of the converter. According to eq. (2.5), the maximum value for L_{m1} can be determined as

$$L_{m1} \leq \frac{{D_{max}}^2 {V_{in-min}}^2}{2P_o f_{sw}} \tag{2.12}$$

where D_{max} is the maximum duty ratio (i.e. 0.5) corresponding to minimum AC input voltage, V_{in-min}. Substituting the parameter values into eq. (2.12) gives

$$L_{m1} \leq \frac{(0.5)^2 \times \left(85\sqrt{2}\right)^2}{2 \times 100 \times 10^5} = 90\ \mu H \tag{2.13}$$

L_{m1} = 90 μH is selected for the prototype converter that is used in simulations and experimental works.

B: Selection of turns ratio of transformer T_1, n_1

Turns ratio of transformer T_1, n_1 determines the voltage level when the converter enters Mode 2, the dual flyback transformer mode, as stated in Section 2.2. It also defines the maximum voltage stress across the main switch as expressed in eq. (2.1). As a result

$$V_{S,max} \leq n_1 V_o + V_{in-max} \tag{2.14}$$

which results in

$$n_1 \leq \frac{V_{S,max} - V_{in-max}}{V_o} \tag{2.15}$$

If the maximum voltage stress on the main switch is considered 500 V, maximum turns ratio of transformer T_1 can be found by substituting appropriate parameter values in eq. (2.15), which gives the following equation:

$$n_1 \leq \frac{500-265\sqrt{2}}{48} = 2.65 \tag{2.16}$$

n_1 = 2.5 is chosen for the transformer T_1 of the prototype converter incorporated in computer simulations and experimental works.

C: Selection of magnetizing inductance of transformer T_2, L_{m2}

L_{m2} needs to be sufficiently high in order to transfer an appropriate amount of energy directly to the output. Low magnetizing inductance of transformer T_2 leads to more direct energy transfer intervals in the converter's operation; more direct energy transfer from transformer T_1 means more low frequency ripple on the output voltage, which is not desirable. Considering eq. (2.9), the minimum value of L_{m2} should be

$$L_{m2} \geq L_{m1}\left(\frac{V_C}{V_{in-min}}\right)^2 \tag{2.17}$$

Substituting the parameter values into eq. (2.17) gives the minimum value for L_{m2}

$$L_{m2} \geq 90 \times 10^{-6} \times \left(\frac{120}{85\sqrt{2}}\right)^2 = 185\ \mu H \tag{2.18}$$

$L_{m2} = 185\ \mu H$ is selected for the prototype converter.

D: Selection of turns ratio of transformer T_2, n_2

The value of n_2 should be low enough to guarantee that the transformer T_2 is fully demagnetized at the end of each line cycle. The turns ratio of transformer T_2 can be selected using the voltage conversion ratio of the converter as in eq. (2.11). To determine the lowest possible value for n_2, low line converter operation should be considered, which means the input voltage is 85 V_{rms}. Substituting the parameter values into eq. (2.11) gives

$$n_2 = \frac{0.5\times 85\sqrt{2}\times\sqrt{180\times10^{-6}}}{48\times(1-0.5)\times\sqrt{2\times90\times10^{-6}}} = 2.5 \tag{2.19}$$

2.4. Conclusion

In this chapter, the single-stage PFC AC/DC converter that is being considered in this thesis, the SSBBDET converter, was discussed. The main advantage of this converter is that its DC bus voltage variation is significantly less than that of other single-stage PFC converters, which allows smaller size components specially DC bus capacitor to be used. This is the result of buck–boost type input section and clamping of V_C to n_1V_o by the secondary winding of T_1. In this chapter, the operation of the converter and its various modes of operation were explained in detail and key component values were selected by a design procedure. These component values were used in a prototype converter from which experimental results were obtained, as will be shown in Chapter 5 of this thesis.

Chapter 3

Averaged State-Space Modeling and Small-Signal Analysis of the Single-Stage PFC Converter

3.1. Introduction

A small-signal state-space model of the Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter is determined in this chapter to be used for designing the voltage and current compensators of the proposed control scheme. In this chapter, the general approach for modeling PWM converters with one inductor operating in Discontinuous Conduction Mode (DCM) is explained and is used to develop a new method of performing averaged state-space modeling for a PWM converter with multiple inductors operating in DCM, such as single-stage PFC converters. The main idea behind this new approach is that the averaged state-space model of a PWM converter with multiple inductors can be derived by first considering each inductor separately using the general averaged state-space model for PWM converters with one inductor, then adding all these separate models to obtain the model for the whole converter. It is shown how a small-signal model and key transfer functions can be extracted from the average state-space model of such a converter. The output to input small-signal transfer functions of the SSBBDET converter are used to keep the small-signal values at zero so that the states of the system can operate at their pre-defined steady-state conditions.

3.2. Averaged State-Space Modeling of PWM Converters with One Inductor Operating in DCM

Several approaches have been proposed to model the dynamic behaviour of PWM converters operating in discontinuous conduction mode (DCM) [63]-[67], with the most popular approach being averaged state-space modeling. The general form of an averaged state-space model is

$$\dot{\bar{x}} = Ax + Bu \tag{3.1}$$

where $\boldsymbol{x}$ is a vector representing the states of the system, $\boldsymbol{u}$ is the vector of the control inputs of the system, and A and B are numerical matrices that are dependent on the parameter values of the converter. In the averaged state-space modeling approach for PWM converters, the averaged current of each inductor and the averaged voltage of each capacitor are considered as the states of the system over a switching cycle. The model is then determined using KCL (Kirchhoff's Current Law) and KVL (Kirchhoff's Voltage Law) equations for the inductors and capacitors.

The input inductor of a low power PWM boost converter like the one shown in Fig. 3.1 generally operates in DCM. In order to develop an averaged state-space model for a DCM PWM converter with one inductor such as the boost converter shown in Fig. 3.1, three time-intervals can be considered for each switching cycle, as indicated by d_1, d_2 and $d_3(= 1 - d_1 - d_2)$ in Fig. 3.2. A piecewise-linear state-space model can be written for each time-interval in a switching cycle as follows:

$$\dot{x} = A_1 x + b_1 v_{in} \qquad \text{for } t \in (0, d_1 T_s) \tag{3.2}$$

$$\dot{x} = A_2 x + b_2 v_{in} \qquad \text{for } t \in (d_1 T_s, (d_1 + d_2) T_s) \tag{3.3}$$

$$\dot{x} = A_3 x + b_3 v_{in} \qquad \text{for } t \in ((d_1 + d_2) T_s, T_s) \tag{3.4}$$

where v_{in} is the only input of the DCM operating PWM converter and T_s is the time period of

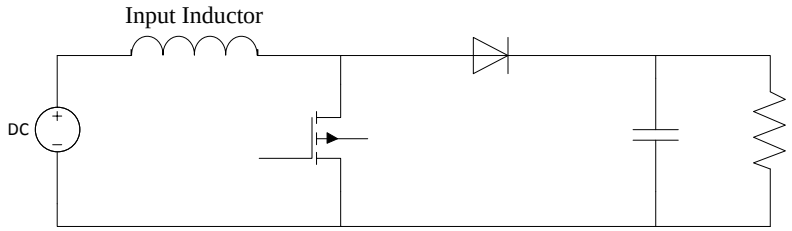


Fig. 3.1 DC/DC Boost Converter

each switching cycle. An averaged state-space model can be applied to equations (3.2) - (3.4) to obtain the averaged model of the converter operating in DCM as

$$\dot{\overline{x}} = [d_1A_1 + d_2A_2 + (1 - d_1 - d_2)A_3]\overline{x} + [d_1b_1 + d_2b_2 + (1 - d_1 - d_2)b_3]v_{in} \quad (3.5)$$

where $\overline{x}$ denotes the average value of the states of the system over a switching cycle. Equation (3.5) is the general form of averaged state-space model of a PWM converter operating in DCM, but the average value for inductor current determined by eq. (3.5) is not necessarily the true average value of the state variable. The average value of the inductor current based on the state-space model, expressed by eq. (3.5) can be compared with the average obtained from the actual value of the charge in the capacitor to determine that eq. (3.5) does not result in a true average value. This can be shown as follows:

Based on the waveform in Fig. 3.2, the average of the input inductor current operating in discontinuous mode over a switching cycle can be written as

$$\overline{i_L} = \frac{i_{Lpk}}{2}(d_1 + d_2) \quad (3.6)$$

where i_{Lpk} is the peak value of inductor current in a switching cycle. Full details on how eq. (3.6) is derived from Fig. 3.1 can be found in Appendix A.

Consider the case in which a capacitor is connected to the input inductor when the switch is on. The averaged state-space model in eq. (3.5) implies that the charging current of the capacitor over a switching cycle, i_{cap-ch}, is $\overline{i_L}d_1$, and substituting eq. (3.6) in it results in

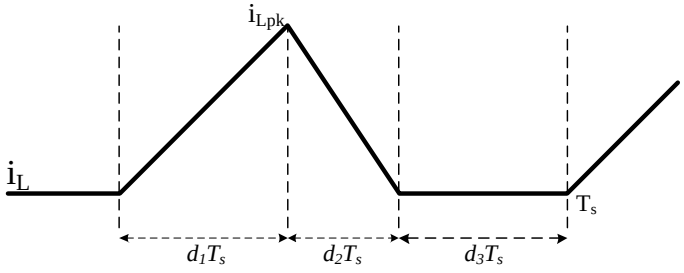


Fig. 3.2 Time intervals of inductor current in a DCM operating converter.

$$i_{cap-ch-ss} = \frac{i_{Lpk} d_1}{2}(d_1 + d_2) \tag{3.7}$$

On the other hand, to obtain the average value of the charging current over the capacitor using KCL expressions, the average charge that the capacitor receives from the inductor in a switching cycle is

$$Q_c = \int_0^{d_1 T_s} i_L(t)\, dt = \frac{i_{Lpk}}{2} d_1 T_s \tag{3.8}$$

which determines the actual average charging current of

$$i_{cap-ch-actual} = \frac{Q_c}{T_s} = \frac{i_{Lpk}}{2} d_1 \tag{3.9}$$

The actual average charging current in eq. (3.9) obtained from the KCL equations is different from the value in eq. (3.7) obtained from averaged state-space model. This implies that the averaged state-space model of eq. (3.5) is somehow deficient in representing the actual behaviour of the PWM converter.

One approach to improving the accuracy of the model is to divide the inductor currents in eq. (3.5) by $(d_1 + d_2)$ as this term is the difference between the actual average value and the average value in the state-space model. In order to divide the inductor currents by $(d_1 + d_2)$ the state vector should be rearranged as $x = \begin{bmatrix} \boldsymbol{i}_L \\ \boldsymbol{v}_C \end{bmatrix}$ where vectors $\boldsymbol{i}_L$ and $\boldsymbol{v}_C$ contain the inductor current and all the capacitor voltages, respectively. The averaged state-space model in eq. (3.5) can then be rewritten as

$$\dot{\overline{x}} = [d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3] \boldsymbol{M} \overline{x} + [d_1 b_1 + d_2 b_2 + (1 - d_1 - d_2) b_3] v_{in} \tag{3.10}$$

in which $\boldsymbol{M}$ is

$$M = \text{diag}\left[\underbrace{\frac{1}{d_1 + d_2}}_{\text{for the inductor current}}, \quad , \underbrace{1,1,\ldots,1}_{\text{number of state capacitors}} \right] \tag{3.11}$$

which now represents the true average value of the inductor.

For the model represented in eq. (3.10) some modifications still need to be made so the model can be used to design the control system of PWM converters with a single inductor that operates in DCM. For such a converter, the only control variable that is used for output voltage regulation is the duty-ratio d_1. This means that d_2 should be replaced by an expression of $d_1$in the averaged state-space model of the converter; the peak value of the inductor current can be used to determine such an expression.

In general, if the voltage across each inductor in a PWM converter is v_{L-on} when the switch is turned on, then using the inductor current equations for the first time-interval (inductors generally store energy during the first time-interval in PWM converters), the peak value of the inductor current can be expressed as

$$i_{Lpk} = v_{L-on} \times \frac{d_1 T_S}{L} \tag{3.12}$$

Substituting this into eq. (3.6) results in

$$d_2 = \frac{2L\overline{i_L}}{d_1 T_S v_{L-on}} - d_1 \tag{3.13}$$

in which d_2 is an expression of d_1 and can be replaced in eq. (3.10). Substituting (3.13) into (3.10) results in the general averaged state-space model of a converter with one inductor operating in DCM as follows:

$$\dot{\overline{x}} = \left[d_1 A_1 + \left(\frac{2L\overline{i_L}}{d_1 T_S v_{L-on}} - d_1\right) A_2 + \left(1 - d_1 - \left(\frac{2L\overline{i_L}}{d_1 T_S v_{L-on}} - d_1\right)\right) A_3\right] \boldsymbol{M}\overline{x} + [d_1 b_1 + \left(\frac{2L\overline{i_L}}{d_1 T_S v_{L-on}} - d_1\right) b_2 + \left(1 - d_1 - \left(\frac{2L\overline{i_L}}{d_1 T_S v_{L-on}} - d_1\right)\right) b_3] v_{in} \tag{3.13A}$$

3.3. Averaged State-Space Modeling of the Single-Stage PFC AC/DC Converter with Direct Energy Transfer

Previously proposed averaged state-space models for PWM converters with multiple inductors can be generally categorized into two major classes:

1) *Reduced-order averaged models* in which one of the inductor currents is eliminated from the final averaged model when there are multiple inductors in the converter structure.

2) *Full-order averaged models* in which all inductor currents and capacitor voltages are retained in the model.

The major drawback of the reduced-order approach when used in the modeling of single-stage PFC AC/DC converters (in which two inductors are used, the input inductor and the magnetizing inductance of the transformer) is the elimination of the input inductor current, which is the main variable to be considered in input current shaping. Full-order models are therefore more accurate than reduced-order models for modeling single-stage PFC converters. A full-order model is developed in this thesis work to model the behaviour of the SSBBDET converter.

The magnetizing inductances of the two transformers (T_1 and T_2) of the SSBBDET converter can be considered as the inductors of the converter and their currents (i_{Lm1}, i_{Lm2}) waveforms are shown in Fig. 3.3. It can be seen from this figure that four time-intervals ($d_1, d_2, d_3, 1 - d_1 - d_2 - d_3$) occur during a switching cycle. The modified averaged state-space model in eq. (3.10) that is generally used to model PWM converters with one inductor in their topology cannot be used in the modeling of the SSBBDET converter. The SSBBDET converter has four time-intervals in a switching cycle (Fig. 3.3), but only three time-intervals are considered in the modified averaged state-space model in eq. (3.10). As a result, a new scheme for modeling the SSBBDET converter is proposed in this section; this scheme is basically a modification of the modified averaged state-space model in eq. (3.10). The main idea behind this new scheme is that the modified averaged state-space model in eq. (3.10) is derived for each inductor in the converter and all

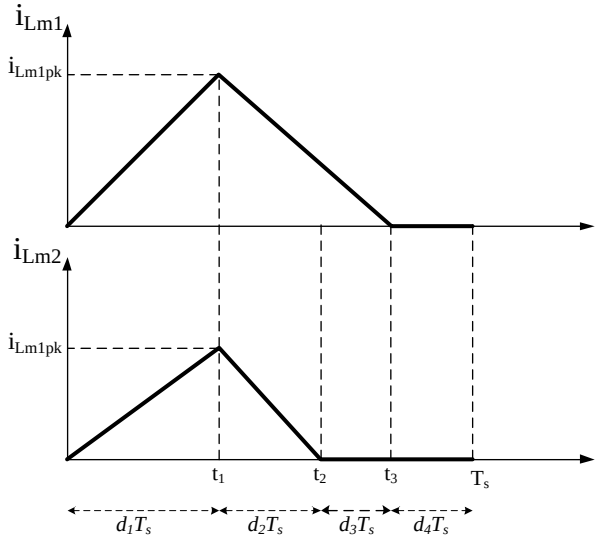


Fig. 3.3 Magnetizing inductances current waveforms.

these derived models are merged together to obtain the averaged state-space model for the SSBBDET converter with multiple inductors that are all operating in DCM.

The currents of the magnetizing inductances (i_{Lm1}, i_{Lm2}) of the transformers (i.e. that are assumed as the inductors of the converter) and the voltages of the capacitors (V_C, V_o) are considered as the states of the converter to be used in the averaged state-space model. According to the operation modes of the converter discussed in Section 2.2, the state equations of the converter for each time-interval can be written as follows:

A: Switch is ON, $0 < t < t_1$

$$L_{m1}\frac{di_{Lm1}}{dt} = V_{inDC} = \frac{2}{\pi}v_{inpk} \tag{3.14}$$

$$L_{m2}\frac{di_{Lm2}}{dt} = v_{C1} \tag{3.15}$$

$$C_o\frac{dV_o}{dt} + \frac{V_o}{R_L} = 0 \tag{3.16}$$

B: Switch is OFF, $t_1 < t < t_2$

$$L_{m1}\frac{di_{Lm1}}{dt} = -n_1 V_o \tag{3.17}$$

$$L_{m2}\frac{di_{Lm2}}{dt} = -n_2 V_o \tag{3.18}$$

$$C_o\frac{dV_o}{dt} + \frac{V_o}{R_L} = n_1 i_{Lm1} + n_2 i_{Lm2} \tag{3.19}$$

C: Switch is OFF, $t_2 < t < t_3$

$$L_{m1}\frac{di_{Lm1}}{dt} = -n_1 V_o \tag{3.20}$$

$$L_{m2}\frac{di_{Lm2}}{dt} = 0 \tag{3.21}$$

$$C_o\frac{dV_o}{dt} + \frac{V_o}{R_L} = n_1 i_{Lm1} \tag{3.22}$$

D: Switch is OFF, $t_3 < t < t_4$

$$L_{m1}\frac{di_{Lm1}}{dt} = L_{m2}\frac{di_{Lm2}}{dt} = C_o\frac{dV_o}{dt} + \frac{V_o}{R_L} = 0 \tag{3.23}$$

In order to use the modified averaged state-space model in eq. (3.13A) for each inductor, matrix ***M*** should be defined. As the average values in equations (3.7) and (3.9) were obtained based on the general current waveform of a DCM operating inductor, these values are also applicable for

any inductor operating in DCM in a PWM converter with multiple inductors such as the SSBBDET converter. As a result matrix $\boldsymbol{M}$ can be rewritten for the SSBBDET converter as follows:

$$M = \text{diag}\left[\underbrace{\frac{1}{d_1+d_2+d_3}, \frac{1}{d_1+d_2}}_{\text{number of state inductors}} , \underbrace{1,1,\dots,1}_{\text{number of state capacitors}}\right] \tag{3.24}$$

which results in:

$$M = \begin{bmatrix} \frac{1}{d_1+d_2+d_3} & 0 & 0 \\ 0 & \frac{1}{d_1+d_2} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3.24A}$$

By substituting equations (3.14) – (3-23) and eq. (3.24A) into eq. (3.10), the averaged state-space equations for each state inductor and state capacitor can be written as follows:

$$\frac{d\overline{i_{Lm1}}}{dt} = \frac{1}{L_{m1}} V_{inDC} d_1 - \frac{n_1 \overline{V_o}}{L_{m1}} (d_2 + d_3) \tag{3.25}$$

$$\frac{d\overline{i_{Lm2}}}{dt} = \frac{1}{L_{m2}} V_C d_1 - \frac{n_2 \overline{V_o}}{L_{m2}} d_2 \tag{3.26}$$

$$\frac{d\overline{V_o}}{dt} = \frac{n_2}{C_o} \overline{i_{Lm2}} \frac{d_2}{d_1+d_2} + \frac{n_1}{C_o} \overline{i_{Lm1}} \frac{d_2+d_3}{d_1+d_2+d_3} - \frac{1}{R_L C_o} \overline{V_o} \tag{3.27}$$

In order to define the modified averaged state-space model in eq. (3.13A), d_2 and d_3 should be defined as an expression of d_1 as it is the only control variable that is used for output voltage regulation. In order to obtain the average values of the inductor currents based on eq. (3.6), the peak values of i_{Lm1} and i_{Lm2} must be determined first; these can be written using eq. (3.12) as follows:

$$i_{Lm1pk} = V_{inDC} \times \frac{d_1 T_s}{L} \tag{3.28}$$

$$i_{Lm2pk} = V_C \times \frac{d_1 T_s}{L} \tag{3.29}$$

and using eq. (3.6) for the average values of the inductor currents results in

$$\overline{i_{Lm1}} = \frac{i_{Lm1pk}}{2} (d_1 + d_2 + d_3) \tag{3.30}$$

$$\overline{i_{Lm2}} = \frac{i_{Lm2pk}}{2}(d_1 + d_2) \tag{3.31}$$

As a result, substituting eq. (3.29) into eq. (3.31) defines d_2 as a function of $d_1$as

$$d_2 = \frac{2L_{m2}\overline{i_{Lm2}}}{d_1 T_s V_C} - d_1 \tag{3.32}$$

then substituting eq. (3.28) and eq.(3.32) into eq. (3.30) gives d_3 as a function of d_1

$$d_3 = \frac{2}{d_1 T_s}\left(\frac{L_{m1}\overline{i_{Lm1}}}{V_{inDC}} - \frac{L_{m2}\overline{i_{Lm2}}}{V_C}\right) \tag{3.33}$$

Substituting eq. (3.32) and eq. (3.33) into equations (3.25) – (3.27) results in

$$\frac{d\overline{i_{Lm1}}}{dt} = \frac{1}{L_{m1}} V_{inDC} d_1 + \frac{n_1}{L_{m1}}\overline{V_o} d_1 - \frac{2n_1\overline{i_{Lm1}}\overline{V_o}}{V_{inDC} T_s d_1} \tag{3.34}$$

$$\frac{d\overline{i_{Lm2}}}{dt} = \frac{1}{L_{m2}} V_C d_1 + \frac{n_2}{L_{m2}}\overline{V_o} d_1 - \frac{2n_2\overline{i_{Lm2}}\overline{V_o}}{V_C T_s d_1} \tag{3.35}$$

$$\frac{d\overline{V_o}}{dt} = \frac{n_1}{C_o}\overline{i_{Lm1}} + \frac{n_2}{C_o}\overline{i_{Lm2}} - \left(\frac{n_2}{C_o}\frac{V_C T_s}{2L_{m2}} + \frac{n_1}{C_o}\frac{V_{inDC} T_s}{2L_{m1}}\right) {d_1}^2 - \frac{1}{R_L C_o}\overline{V_o} \tag{3.36}$$

In single-stage PFC AC/DC converters, d_1 is the only variable that can be used to regulate the output voltage and shape the input current. On the other hand, the only controllable variables in averaged state-space models are the inputs of the system. As can be seen in equations (3.34) – (3.36), $d_1$appears as a parameter in matrix A and can be used as a control variable if it is separated from this matrix and placed as an input of the system. To separate $d_1$from the matrix, a linearization method in which a multivariable function is linearized around an equilibrium point is used. For example, the linearization equation around the equilibrium point of (a, b) for a two-variable function f(x, y), can be written as

$$\mathrm{f}(x, y) \approx \mathrm{f}(a, b) + \left.\frac{\partial \mathrm{f}(x,y)}{\partial x}\right|_{a,\,b} \tilde{x} + \left.\frac{\partial \mathrm{f}(x,y)}{\partial y}\right|_{a,\,b} \tilde{y} \tag{3.37}$$

where $\tilde{x}(= x - a)$ and $\tilde{y}(= y - b)$ are small-signal values of x and y, respectively.

For the SSBBDET converter, the equilibrium point can be determined by solving averaged state-space equations (3.34) – (3.36) when $\dot{\overline{x}} = 0$. To obtain a solution for these equations, the following parameter values obtained in Chapter 2 can be substituted into equations (3.34) – (3.36):

- $L_{m1} = 85\ \mu H$, $L_{m2} = 194\ \mu H$
- $n_1 = n_2 = 2.5$
- $C = 560\ \mu F$, $C_o = 470\ \mu F$
- $R_L = 25.48\ \Omega$
- $T_s = 10\ \mu s$, $D = 22.22\ \%$
- $V_{inDC} = 190.918\ V$
- $V_C = 157.48\ V$ (3.38)

Solving $\dot{\bar{x}} = 0$, the equilibrium point of the previously discussed single-stage converter can be determined to be

- $i_{Lm1} = 1.2701\ A$
- $i_{Lm2} = 0.4137\ A$
- $V_o = 59.1727\ V$ (3.39)

The linearization equation (3.37) can be applied to each multivariable term in the averaged state-space equations (3.34) – (3.36) by using the values in eq. (3.38) and eq. (3.39). As a result, the small-signal state-space equations of the converter can be derived as follows:

$$\frac{d\tilde{\imath}_{Lm1}}{dt} = -5.3233 \times 10^5 \tilde{\imath}_{Lm1} - 1.105 \times 10^4 \tilde{v}_o + 7.1466 \times 10^6 \tilde{d}_1 \quad (3.40)$$

$$\frac{d\tilde{\imath}_{Lm2}}{dt} = -6.4536 \times 10^5 \tilde{\imath}_{Lm2} - 3.994 \times 10^3 \tilde{v}_o + 2.7866 \times 10^6 \tilde{d}_1 \quad (3.41)$$

$$\frac{d\tilde{v}_o}{dt} = 5.32 \times 10^6 \tilde{\imath}_{Lm1} + 5.32 \times 10^6 \tilde{\imath}_{Lm2} - 83.5031 \tilde{v}_o - 0.08134 \times 10^6 \tilde{d}_1 \quad (3.42)$$

It should be noted that since the input voltage is assumed to be constant during each switching cycle, its small-signal value is considered to be zero in the small-signal state-space model of the converter.

In a converter represented by linearized small-signal state-space model, these small-signal values of the states have to be kept at zero to maintain the converter in its pre-defined steady-state condition. As a result, the small-signal state-space model and the small-signal transfer functions (output to input) of the converter should be considered to design the controller for the SSBBDET converter.

The small-signal state-space model of the converter can be derived based on eq. (3.13A) using equations (3.40) – (3.42) as follows:

$$\dot{\tilde{x}} = \begin{bmatrix} -5.3233 \times 10^5 & 0 & -1.1050 \times 10^4 \\ 0 & -6.4536 \times 10^5 & -3.9940 \times 10^3 \\ 5.32 \times 10^6 & 5.32 \times 10^6 & -83.5031 \end{bmatrix} \begin{bmatrix} \tilde{\imath}_{Lm1} \\ \tilde{\imath}_{Lm2} \\ \tilde{v}_o \end{bmatrix} + \begin{bmatrix} 7.1466 \times 10^6 \\ 2.7866 \times 10^6 \\ -0.08134 \times 10^6 \end{bmatrix} \tilde{d}_1 \tag{3.43}$$

In order to derive the small-signal transfer functions of the converter (outputs to the input), the outputs of the system should be defined. In a small-signal state-space model, the outputs are defined by

$$\tilde{y} = C\tilde{x} + D\tilde{u} \tag{3.44}$$

For the SSBBDET converter, these outputs are the output voltage and the input current of the converter since the control system is designed for these variables. To determine the outputs in eq. (3.44), the following considerations should be made:

1) The output voltage is also one of the states of the system.
2) The input current is equal to i_{Lm1} in the first time-interval and is zero for the rest of the switching cycle. $(i_{in} = i_{Lm1}.d_1)$

Using linearization equation (3.36) with equations (3.38) and (3.39), the small-signal state-space equations for the outputs can be written as

$$\begin{bmatrix} \tilde{v}_o \\ \tilde{\imath}_{in} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0.222 & 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{\imath}_{Lm1} \\ \tilde{\imath}_{Lm2} \\ \tilde{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 1.2701 \end{bmatrix} \tilde{d}_1 \tag{3.45}$$

Equations (3.43) and (3.45) are the small-signal state-space representation of the SSBBDET converter and can be used to derive the output to input transfer functions.

In order to derive the output to duty ratio transfer functions of the system, a frequency domain representation of the converter should be obtained by applying the Laplace transform to equations (3.43) and (3.45); this yields

$$\frac{\boldsymbol{Y}(s)}{D_1(s)} = \boldsymbol{C}(s\boldsymbol{I}_3 - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D} \tag{3.46}$$

where $\boldsymbol{I}_3$ is the 3-by-3 identity matrix, s is the Laplace operator and $\boldsymbol{Y}(s)$ and $D_1(s)$ are the Laplace transforms of the output vector (control outputs) and duty ratio (control input), respectively.

Based on equations (3.43) and (3.45), matrices ***A, B, C*** and ***D*** can be determined as follows:

$$\boldsymbol{A} = \begin{bmatrix} -5.3233 \times 10^5 & 0 & -1.1050 \times 10^4 \\ 0 & -6.4536 \times 10^5 & -3.9940 \times 10^3 \\ 5.32 \times 10^6 & 5.32 \times 10^6 & -83.5031 \end{bmatrix}$$

$$\boldsymbol{B} = \begin{bmatrix} 7.1466 \times 10^6 \\ 2.7866 \times 10^6 \\ -0.08134 \times 10^6 \end{bmatrix}$$

$$\boldsymbol{C} = \begin{bmatrix} 0 & 0 & 1 \\ 0.222 & 0 & 0 \end{bmatrix}$$

$$\boldsymbol{D} = \begin{bmatrix} 0 \\ 1.2701 \end{bmatrix} \tag{3.47}$$

Substituting matrices in eq. (3.47) into eq. (3.46) results in the output to control (duty ratio) small-signal transfer functions

$$\frac{\tilde{V}_o(s)}{D(s)} = \frac{-8.134\times10^4 s^2 + 5.2748\times10^{13} s + 3.24\times10^{19}}{s^3 + 1.1778\times10^6 s^2 + 4.2368\times10^{11} s + 4.9278\times10^{16}} \tag{3.48}$$

$$\frac{\tilde{I}_{in}(s)}{D(s)} = \frac{1.2701 s^3 + 3.0838\times10^6 s^2 + 1.5632\times10^{12} s + 6.0144\times10^{16}}{s^3 + 1.1778\times10^6 s^2 + 4.2368\times10^{11} s + 4.9278\times10^{16}} \tag{3.49}$$

in which the variation in the input voltage during each switching cycle is ignored. These transfer functions can be used to keep small-signal values of the output voltage and input current at zero so the converter can work at its pre-defined steady-state condition.

3.4. Conclusion

A small-signal state-space model of the SSBBDET converter based on a new averaged state-space model was determined in this chapter. Conventional approaches fail to accurately model the behaviour of single-stage PFC converters such as the SSBBDET converter because of multiple inductors in their structure (the magnetizing inductances of transformers). A new

scheme for the averaged state-space modeling of a single-stage PFC converter with multiple inductors was proposed based on the modification of conventional approach for PWM converters with one inductor. The main idea behind this new scheme is that the general averaged state-space model for PWM converters with one inductor can be applied to each inductor separately and then all these separate models can be merged together to form the averaged state-space model for the SSBBDET converter. A small-signal state-space model and output to duty ratio small-signal transfer functions of the converter was extracted from the new averaged state-space model. This model and the transfer functions will be are used later in this thesis to keep the small-signal values at zero so the converter can operate at its pre-defined steady-state condition.

Chapter 4

New Control Scheme for Single-Stage PFC AC/DC Converters Employing Direct Energy Transfer

4.1. Introduction

A control strategy for the Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter presented in Chapter 2 is proposed in this chapter. In this chapter, the conventional average current mode control approach that is generally used for single-stage PFC converters is discussed and its drawbacks are reviewed. A new control strategy based on conventional average current mode technique is introduced and a mathematical analysis of this technique is performed. The results of this analysis are used to select appropriate parameter values that ensure the proper operation of the SSBBDET converter with the new control scheme.

4.2. Limitation of Conventional Average Current-Mode Control Structure for the Proposed Single-Stage PFC Converter

Figure 4.1 shows a general diagram of the SSBBDET converter, implemented with the average current mode technique described in Section 1.5.3, which is the most popular control method used for single-stage PFC converters. In this technique, two control feedback loops, one for the output voltage and one for the input current, are connected in cascade with each other. The inner feedback loop is an input current feedback loop that makes the input current track the current reference signal as much as possible during each switching cycle. The outer feedback loop is an output voltage feedback loop that regulates the output voltage.

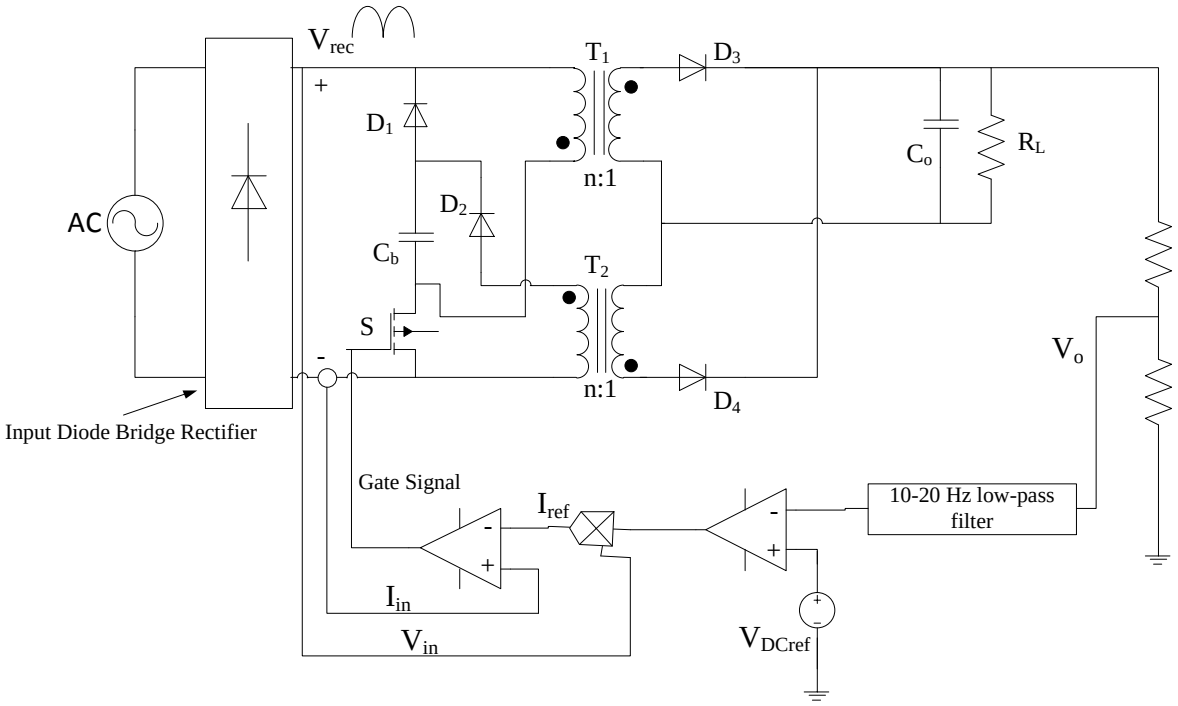


Fig. 4.1 Single-stage PFC converter with conventional average current-mode control.

In order to achieve a high input power factor, the current reference signal must be in phase with the input voltage. This can be ensured by generating the current reference signal from the product of the output of voltage feedback loop (which determines the amplitude of current reference signal) and the input voltage (which can be used as a template to determine the phase of the current reference signal relative to the input voltage and to determine the shape of the current). In order to minimize the effect that the two feedback loops may have on each other, the bandwidth of each loop should be set so that it does not overlap with that of the other loop. The bandwidth considerations of each loop can be summarized as follows:

- *Input current feedback loop bandwidth:* The function of the current feedback loop compensator is to make the input current follow the current reference during each switching cycle. As a result, the current loop bandwidth must be higher than the voltage loop bandwidth since more precise tracking is required and a bandwidth of 8 – 10 kHz is usually set for the current feedback loop [73]. It should be noted that it is not the input current waveform itself that is actually used to track the current reference, but a rectified version of it, with the negative portion of the original waveform flipped over to become positive so that

the reference that is actually used is a 120 Hz waveform consisting of positive sinusoidal humps.

- *Output voltage feedback loop bandwidth:* As mentioned in Chapter 2, when the converter is operating under high line conditions, it is very likely that the DC bus voltage will try to exceed the pre-set voltage limit so that the input flyback transformer will directly transfer energy to the output. Since the voltage and current waveforms at the output of the diode bridge rectifier are rectified sinusoidal signals, they will have a 120 Hz component. This 120 Hz component will appear as a similar component of the same frequency at the output, which can be reduced by increasing the amount of the output capacitance, but this will result in a very slow dynamic response [71] - [72]. If a 10-20 Hz low-pass filter is added to voltage feedback loop to make the bandwidth of the output voltage feedback loop low, then a faster response can be achieved, but it will still be sluggish.

The major drawback of the average mode control scheme shown in Fig. 4.1 is the sluggish converter transient response due to the presence of a low-pass filter in the output voltage feedback loop. Increasing the bandwidth of voltage feedback loop to make the response faster, however, causes a considerable 120 Hz voltage ripple component to appear in the output of voltage feedback loop. This 120 Hz ripple component can distort the input current reference waveform and thus ultimately distort the input current waveform as well. This distortion in the line current may be so significant that the single-stage PFC converter may not comply with harmonic standards like EN61000-3-2. As a result, another control scheme is needed for the SSBBDET converter.

4.3. A Control Strategy for the Single-Stage PFC Converter with Direct Energy Transfer

In this section, a new control scheme is proposed for the SSBBDET converter. Before introducing the new control scheme, the basic principles behind it is reviewed here first. The SSBBDET converter can have considerable output voltage ripple when it is operating at high input line voltages because this is when the mechanism used to clamp the voltage across capacitor C_b, transformer T_1 and diode D_3, is most likely to be active. When the clamping mechanism is active, energy is transferred away from C_b to the output so that C_b is not charged

above the clamping limit, which is set by the turns ratio of T_1. Since the voltage of the input diode rectifier bridge and the current flowing out of it are rectified sinusoidal waveforms, each with a significant 120 Hz component, a 120 Hz component will also be superimposed on top of the output voltage as a result of the link between input and output sections due to T_1 and D_3 clamping mechanism. As a result, the output capacitor C_o must be made larger to try to filter out the 120 Hz component to make the output voltage as flat and as purely DC; this increases converter size and slows down converter transient response.

Since the 120 Hz component that appears at the output is most significant when the input current is sinusoidal, it can be reduced if the input current reference is intentionally distorted so that the input current is distorted as well. The main idea behind this approach is that decreasing the pulsating output power leads to output voltage ripple reduction. Since there is a balance between the pulsating input power and pulsating output power, this can be done by decreasing the pulsating input power. One solution to reduce the pulsating input power is to distort the input current.

Since the input current is intentionally distorted in a way that allows the input current to approximate the reference waveform that would result if a fast voltage loop without filtering is implemented in the conventional scheme, the converter can track the reference with a faster response. This is because of its natural and inherent tendency to follow the reference as quickly as possible. This is to be contrasted with the fact that the converter becomes unstable if the conventional average current mode approach is implemented without a low-pass filter.

The main idea behind the proposed scheme is to intentionally distort the input current reference in an appropriate manner so that the output voltage ripple can be significantly reduced. The proposed scheme is a modified version of the conventional average current mode control technique and is based on the work that was presented in [68], which first introduced the concept of input current distortion that is the main focus of this work. The main difference between the proposed scheme and the one proposed in [68] is that the converter under study for this work is a single-stage PFC converter with a buck-boost input section while the converter examined in [68] was an AC/DC boost converter. As a result, some changes must be made in the analysis and implementation of the control scheme from [68] for the converter studied in this work.

It should be noted that the implementation of the proposed control approach to the SSBBDET converter results in a single-stage converter with a fixed primary-side DC bus voltage (voltage across capacitor C_b in Fig. 4.1), an improved dynamic response to load and line variations with little output voltage ripple, and an input current harmonic content that can comply with EN 61000-3-2 Class D standards. No previously proposed single-stage converter has this combination of features.

A. Control Scheme Analysis

In order to define the exact amount of harmonic distortion that must be introduced into the input current, the effect of the output voltage ripple on the input current waveform must be analyzed. The first step is to assume that the input voltage and input current of the power stage in Fig. 4.1 are as follows:

$$v_{in}(t) = V_{inp}|\sin \omega_L t| \tag{4.1}$$

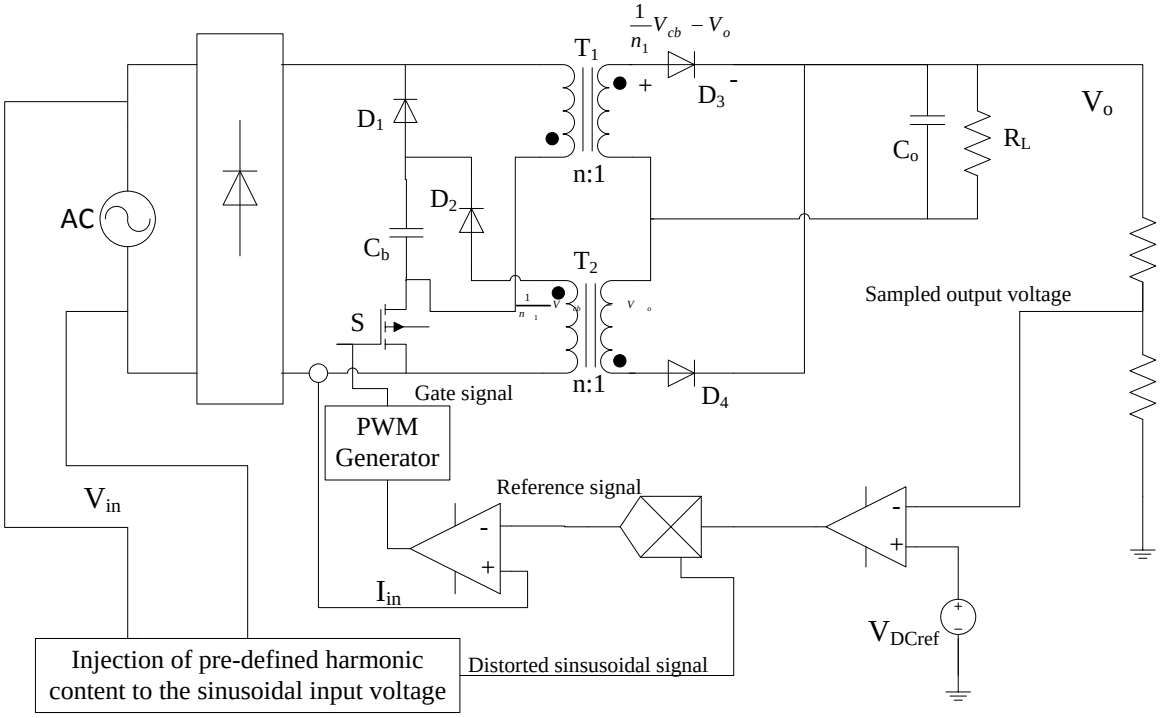


Fig. 4.2 Proposed control strategy on the single-stage PFC converter.

$$i_{in}(t) = \frac{V_{inp}|\sin \omega_L t| v_A(t)}{K_{CC}} \tag{4.2}$$

where V_{inp} is peak amplitude of input voltage, ω_L is the angular frequency of the line, v_A is output of the voltage feedback loop and K_{CC} is a constant determined by the current loop controller to compensate for the amplitude of input current. Note that the input current reference signal is dependent on the product of the output of voltage feedback loop, v_A (which determines the amplitude of current reference signal), and the input voltage (which is used as a template to determine the phase of the current reference signal relative to the input voltage and to determine the shape of the current).

If the low-pass filter is eliminated, then voltage $v_A(t)$ will have more ripple and this will affect $i_{in}(t)$. Eliminating the low-pass filter in the voltage feedback loop allows voltage $v_A(t)$ to be written as

$$v_A(t) = v_{Adc} + v_{Aac}(t) \tag{4.3}$$

$$v_{Aac}(t) = v_{Aacp} \sin(2\omega_L t - \phi_L) \tag{4.4}$$

where v_{Adc} is the DC error of output voltage, v_{Aac} is the AC component of the output voltage, v_{Aacp} is the peak amplitude of v_{Aac} and $\phi_L$is its phase lag angle as defined by the delay time of the controller (i.e. if the delay time is assumed to be t_d then ϕ_L is $2\omega_L t_d$). Note that only the frequency component that is twice the line frequency (the 120 Hz component) is considered in the output voltage ripple as this component is the only significant harmonic in the voltage ripple of the SSBBDET converter.

The next step in trying to determine the effect of the output voltage ripple on the input current waveform is to determine the output voltage ripple components. The output voltage is the product of the output impedance and the output current ($v_o(t) = Z_{R_L \| C_o} i_o(t)$, where $Z_{R_L \| C_o}$is the impedance of the output stage). As a result, the output voltage ripple is proportional to the output current ripple. For the purpose of simplicity, the output current ripple is considered instead of the output voltage ripple. Therefore, In order to determine the output voltage ripple, the output current waveform and its harmonic components should be determined at first.

The instantaneous input power, $p_{in}(t)$, is a product of $v_{in}(t)$ in eq. (4.1) and $i_{in}(t)$ in eq. (4.2) and can be expressed as

$$p_{gi}(t) = v_{in}(t).i_{in}(t) = \frac{V^2{}_{inp}}{K_{CC}} v_A(t) \sin^2(\omega_L t) \tag{4.5}$$

Substituting equations (4.3) and (4.4) into (4.5) gives

$$p_{gi}(t) = \frac{V^2{}_{inp} v_{Adc}}{K_{CC}} \sin^2(\omega_L t)\,(1 + k_v \sin(2\omega_L t - \phi_L)) \tag{4.6}$$

where k_v is the ratio of the peak amplitude of the AC component of v_A to its DC component and can be expressed as

$$k_v = \frac{v_{Aacp}}{v_{Adc}} \tag{4.7}$$

Like the instantaneous input power, the instantaneous output power can be determined by multiplying the output voltage V_o and the output current i_o as follows:

$$p_{oi} = V_o.i_o(t) \tag{4.8}$$

Assuming that the converter is ideal and has no power losses, equating the instantaneous input power and instantaneous output power (i.e. $p_{gi} = p_{oi}$) results in

$$i_o(t) = \frac{V^2{}_{inp} v_{Adc}}{V_o K_{CC}} \sin^2(\omega_L t)\,(1 + k_v \sin(2\omega_L t - \phi_L)) \tag{4.9}$$

v_{Adc} is the DC error of the output voltage and is uncontrollable. Since the main purpose is to control the output voltage ripple and the input line current, the output current and the input current expressions have to be independent of v_{Adc}.

With the instantaneous output current determined in (4.9), the next step is to express the output current waveform independent of v_{Adc}. This can be done by considering the average input power and output power. The average value of the input power, p_{gav} in a half line cycle can be written as

$$p_{gav} = \frac{2}{T_L} \int_0^{\frac{T_L}{2}} p_{gi}(t)\,dt = \frac{V^2{}_{inp} v_{Adc}}{4K_{CC}} (2 + k_v \sin\phi_L) \tag{4.10}$$

where T_L is the line time period. The average DC output power delivered to the load is

$$p_o = \frac{{V_o}^2}{R_L} \tag{4.11}$$

Equating the average input power and DC output power results in

$$V_{inp} = \frac{4K_{CC}{V_o}^2}{R_L v_{Adc} V_{inp}} \frac{1}{(2+k_v \sin\phi_L)} \tag{4.12}$$

Considering eq. (4.12), the output current in eq. (4.9) can be rewritten as

$$i_o(t) = \frac{4V_o}{R_L} \frac{(1+k_v \sin(2\omega_L t-\phi_L))}{(2+k_v \sin\phi_L)} \sin^2(\omega_L t) \tag{4.13}$$

Equation (4.13) describes the output current of the converter. It will be used later to determine the relative amplitude of the output voltage ripple.

While the output current is required for measurement of the output voltage ripple, input current is also needed for measuring the harmonic distortion. Substituting equations (4.12), (4.3) and (4.4) into eq. (4.2) results in the following expression for the line input current, $i_{inL}(t)$:

$$i_{inL}(t) = \frac{4{V_o}^2}{R_L V_{inp}} \frac{(1+k_v \sin(2\omega_L t-\phi_L))}{(2+k_v \sin\phi_L)} \sin(\omega_L t) \tag{4.14}$$

Equation (4.14) describes the input current when the low-pass filter in the voltage feedback loop is eliminated, which improves the transient response of the converter, but leads to harmonic distortion in the input current. As can be seen in eq. (4.14), parameters k_v and $\phi_L$have a strong influence on the input current waveform and thus on its harmonic contents.

The harmonic contents of the input current and output current can be written by separating the harmonic component frequencies from equations (4.13) and (4.14):

$$i_{inL}(t) = i_{inL1}(t) + i_{inL3}(t) \tag{4.15}$$

$$i_o(t) = i_{odc} + i_{o2}(t) \tag{4.16}$$

where $i_{inL1}(t)$ is the main component with the frequency of 60 Hz (line frequency, f_{line}), $i_{inL3}(t)$ is the third harmonic component with the frequency of 180 Hz (three times the line

frequency, $3f_{line}$), i_{odc} is the DC value of the output current and $i_{o2}(t)$ is the ripple component of the output current (and the output voltage) with the frequency of 120 Hz (twice the line frequency, $2f_{line}$). The harmonic components of equations (4.15) and (4.16) can be written as follows:

$$i_{inL1}(t) = \frac{4{V_o}^2}{R_L V_{inp}(2+k_v \sin\phi_L)}\left[\sin(\omega_L t) - \frac{k_v}{2}\cos(\omega_L t - \phi_L)\right] \tag{4.17}$$

$$i_{inL3}(t) = \frac{2{V_o}^2 k_v}{R_L V_{inp}(2+k_v \sin\phi_L)}\cos(3\omega_L t - \phi_L) \tag{4.18}$$

$$i_{odc} = \frac{V_o}{R_L} \tag{4.19}$$

$$i_{o2}(t) = \frac{2V_o}{R_L(2+k_v \sin\phi_L)}[k_v \sin(2\omega_L t - \phi_L) - \cos(2\omega_L t)] \tag{4.20}$$

To find the change in the input current distortion while the low-pass filter is added to voltage feedback loop, input current expression should be incorporated with the filtering considered. In this case, the input voltage and current of the power stage can be written as

$$v_{in}(t) = V_{inp}|\sin\omega_L t| \tag{4.21}$$

$$i_{in}(t) = \frac{V_{inp}V_A|\sin\omega_L t|}{{K'}_{CC}} \tag{4.22}$$

where V_A (i.e. the voltage error) is a DC value due to use of a low-pass filter in the voltage loop. It should be noted again that the input voltage assumed as the input current reference in these equations. Multiplying equations (4.21) and (4.22) gives the instantaneous input power as

$$p_{gi}(t) = \frac{{V_{inp}}^2 V_A}{{K'}_{CC}}\sin^2(\omega_L t) \tag{4.23}$$

To determine the input current independently of V_A, similar to what was done for the case without the low-pass filter, the balance between average input and output powers should be considered. The average input power over a half line cycle can be expressed as follows:

$$p_{gav} = \frac{2}{T_L}\int_0^{\frac{T_L}{2}} p_{gi}(t)\,dt = \frac{{V^2}_{inp}V_A}{2{K'}_{CC}} \tag{4.24}$$

The DC output power is the same as eq. (4.11). Equating the average input power and the DC output power results in

$$\frac{V^2{}_{inp}V_A}{V_o K'_{CC}} = \frac{2V_o}{R_L} \tag{4.25}$$

Substituting eq. (4.25) into equations (4.22) gives

$$i_{in}(t) = \frac{2{V_o}^2}{V_{inp}R_L}|\sin \omega_L t| \tag{4.26}$$

Based on eq. (4.26), the input line current can be written as

$$i_{inL}(t) = \frac{2{V_o}^2}{V_{inp}R_L}(\sin \omega_L t) \tag{4.27}$$

According to equations (4.15) and (4.16), the harmonic contents of input current can be written as follows:

$$i_{inL1}(t) = \frac{2{V_o}^2}{V_{inp}R_L}(\sin \omega_L t) \tag{4.28}$$

$$i_{inL3}(t) = 0 \tag{4.29}$$

Considering eq. (4.14) as the input line current when the low-pass filter is eliminated (which leads to improved transient response and undesirable input current distortions), and eq. (4.27) as the input line current with the low-pass filter in control loop (which has slow transient response and acceptable input current distortion), it can be understood that if the input current reference in the second case is assumed to be

$$i_{ref\_tmp} = \frac{2}{(2+k_v \sin \phi_L)}(1 + k_v \sin(2\omega_L t - \phi_L))v_{in}(t) \tag{4.30}$$

which basically can be determined by dividing eq. (4.14) to eq. (4.28). As a result, the input line current can be rewritten as

$$i_{inL}(t) = \frac{4{V_o}^2}{R_L V_{inp}} \frac{(1+k_v \sin(2\omega_L t - \phi_L))}{(2+k_v \sin \phi_L)} \sin(\omega_L t) \tag{4.31}$$

This is exactly the same equation as eq. (4.14) except that the harmonic distortion in this case is intentionally injected into the reference signal and is controlled.

B. Control Scheme Design

In order to select values for parameters k_v and ϕ_L that will result in an appropriately distorted input current waveform, some harmonic standard must be considered. For this work, the EN61000-3-2 Class D harmonic standard is considered as it is the most widely used standard for converters like SSBBDET converter. The amplitude of the third input current harmonic can be determined in eq. (4.18) and can be written as

$$i_{inL3p}(t) = \frac{2{V_o}^2 k_v}{R_L V_{inp}(2+k_v \sin\phi_L)} \tag{4.32}$$

Substituting eq. (4.11) into eq. (4.32) results in

$$i_{inL3p}(t) = \frac{2p_{gav}}{V_{inp}} \frac{k_v}{(2+k_v \sin\phi_L)} \tag{4.33}$$

According to the EN61000-3-2 Class D standard, the limit on the amplitude of each harmonic in the input current is proportional to the converter's input power and the ratio of the amplitude of third harmonic to the rms value of average input power should be less than 3.4 mA/W. This can be expressed as

$$\frac{i_{inL3p}(t)}{\sqrt{2}p_{gav}} = \frac{\sqrt{2}}{V_{inp}} \frac{k_v}{(2+k_v \sin\phi_L)} \leq 3.4 \times 10^{-3} \tag{4.34}$$

This inequality can be evaluated by different values of k_v and ϕ_L. Fig. 4.3 indicates the

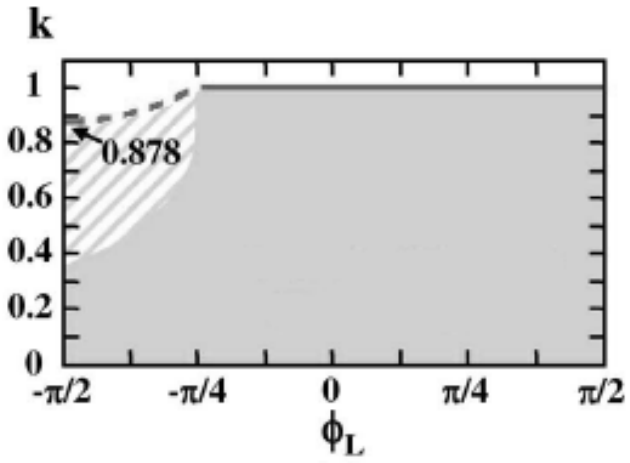


Fig. 4.3 Area of compliance (grey area) for the SSBBDET converter.

compliance area (the grey area) which is a graph of k_v for different values of ϕ_L. According to eq. (4.34), the converter does not comply with the harmonic standard when ϕ_L is between $-90°$ and $-45°$ and k_v is higher than 0.87 at the same time.

The output voltage ripple amplitude is proportional to the output current ripple amplitude in eq. (4.20) and can be written as

$$i_{o2p} = \frac{2V_o}{R_L}\frac{\sqrt{1+{k_v}^2+2k_v \sin\phi_L}}{2+k_v \sin\phi_L} \tag{4.34}$$

To find appropriate values for k_v and ϕ_L, these parameters should be such that the output current ripple amplitude in eq. (4.34) is as low as possible. Fig. 4.4 shows the relative output voltage ripple amplitude for different acceptable values of k_v and ϕ_L. As indicated in this figure, when $\phi_L = -90°$ and k_v=0.87, a minimum output voltage ripple amplitude can be achieved. It should be noted that k_v cannot exceed this value because it will exit the compliance area. By substituting these values into eq. (4.30), the input current reference signal can be expressed as

$$i_{ref\_tmp} = \frac{2}{1.13}\left(1 + 0.87 \sin\left(2\omega_L t + \frac{\pi}{2}\right)\right) v_{in}(t) \tag{4.35}$$

Note that as the term $\frac{2}{1.13}$ is a constant value, it can be considered in the compensator gain K_{CC} in the current feedback loop and eliminated from the reference signal. As a result, the reference

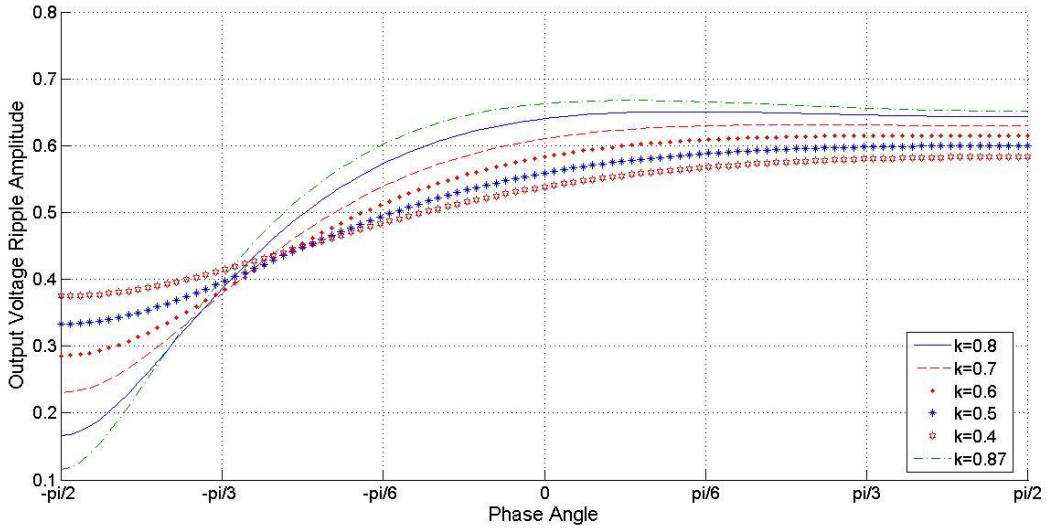


Fig. 4.4 Relative Output voltage ripple amplitude for different designs of PFC converter.

signal for the input current for this new control scheme can be written as follows:

$$i_{refds} = v_{inp}\left(1 + 0.87\sin\left(2\omega_L t + \frac{\pi}{2}\right)\right)\sin(\omega_L t) \tag{4.36}$$

To generate this reference signal, a phase lock loop (PLL) needs to be incorporated into the control scheme to extract the input voltage phase and thus the input current in phase with the input voltage.

As shown in eq. (4.10), v_{Adc} (DC error of output voltage) depends on the square value of the peak amplitude of the input voltage for a given average input power. Since the single-stage converter under study operates with a universal line input voltage range (85 Vrms – 265 Vrms), a feedforward loop should be added to the input current reference signal generator to compensate for line voltage variation effects on the voltage feedback loop [74]. Fig. 4.5 shows the designed control scheme for the SSBBDET converter with the input current reference signal generator and the feedforward loop. As shown in this figure, the pulsating input power in this case can be

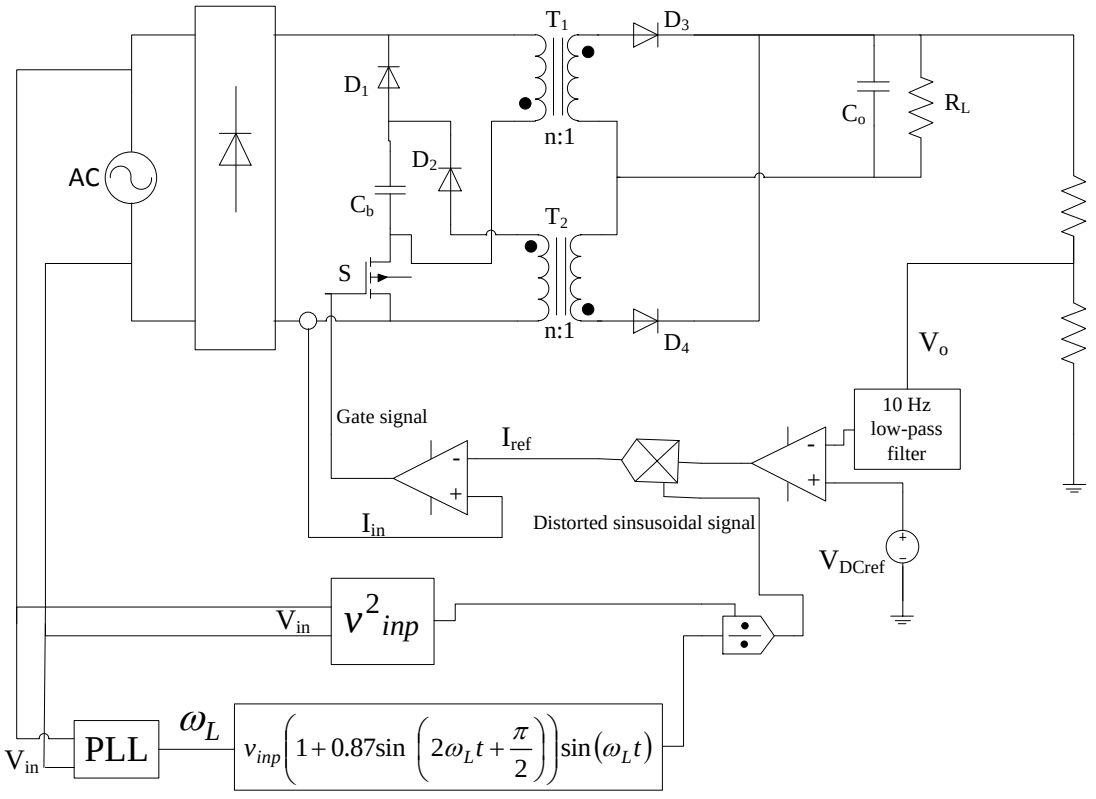


Fig. 4.5 Designed control scheme for the single-stage PFC converter employing direct energy transfer.

written as

$$p_{gi}(t) = \frac{v_{Adc}}{K_{CC}} \sin^2(\omega_L t)\,(1 + k_v \sin(2\omega_L t - \phi_L)) \tag{4.37}$$

The dependency of v_{Adc} and the voltage feedback loop on the input voltage peak amplitude is now eliminated.

The block diagram of the designed control system is shown in Fig. 4.6. K_{vo}, K_{iin}, K_{vin} are the gains of the sensing circuits, and $G_{v_o d}$ and $G_{v_o i_{in}}$ are the transfer functions of the converter that were derived in Chapter 3 and can be written as follows:

$$G_{v_o d} = \frac{V_o(s)}{D(s)} = \frac{-8.134\times10^4 s^2 + 5.2748\times10^{13} s + 3.24\times10^{19}}{s^3 + 1.1778\times10^6 s^2 + 4.2368\times10^{11} s + 4.9278\times10^{16}} \tag{4.38}$$

$$G_{v_o i_{in}} = \frac{V_o(s)}{I_{in}(s)} = \frac{V_o(s)}{D(s)} \times \frac{D(s)}{I_{in}(s)} = \frac{-8.134 \times 10^4 s^2 + 5.2748 \times 10^{13} s + 3.24 \times 10^{19}}{1.2701 s^3 + 3.0838 \times 10^6 s^2 + 1.5632 \times 10^{12} s + 6.0144 \times 10^{16}} \tag{4.39}$$

As previously discussed, the bandwidth of the voltage loop compensator is designed to be 10 Hz and the bandwidth of the current loop compensator is selected to be 10 kHz. Unlike with the conventional control scheme, having a voltage loop with a 10 Hz bandwidth does not result in a sluggish transient response because the current reference signal is designed in a way that the transient response is exactly the same as the case without any filtering in the voltage loop.

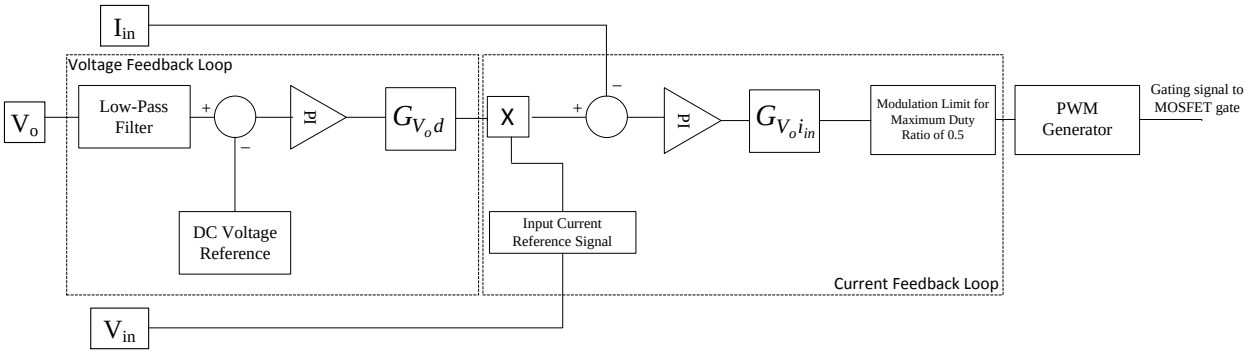


Fig. 4.6 Block diagram of the designed control system.

4.4. Conclusion

A control strategy for the single-stage PFC presented in Chapter 2 was proposed in this chapter. In this chapter, the conventional average current mode control approach for single-stage PFC converters was discussed and it was explained that it results in very slow converter transient response. The proposed control scheme was proposed to address this issue by purposefully distorting the input current reference in the conventional average current mode approach. A mathematical analysis of this technique is performed and the results of this analysis were used to select appropriate parameter values that ensure the proper operation of the SSBBDET converter with the new control scheme. The parameters that were selected were implemented in a prototype converter that was implemented with the proposed control scheme. The experimental results that were obtained from this prototype will be discussed in the following chapter of this thesis.

Chapter 5

Experimental Results of the Single-Stage PFC AC/DC Converter with Proposed Control Scheme

5.1. Introduction

In this chapter, experimental results obtained from a prototype of the SSBBDET converter, implemented with the proposed control scheme described in the previous chapter, are presented. The converter was implemented with the design parameters that were determined in previous chapters of this thesis. The parameters for the actual converter circuit were determined in Chapter 2 while those for the control scheme were determined in Chapters 3 and 4. It is confirmed that the converter can operate with an excellent transient response and an acceptable input current harmonic content when implemented with the new control scheme.

5.2. Experimental Results of the Implemented Single-Stage PFC Converter

An experimental prototype of the SSBBDET converter was implemented with the proposed control scheme described in the previous chapter. According to the design procedure presented in Chapter 2, the prototype was implemented with the following specifications:

- Input voltage 85 ~ 265 V_{rms}
- Output voltage 48 V_{dc}
- Switching frequency 100 kHz
- Maximum output power 100 W

The two transformers had magnetizing inductances of L_{m1}=194 μH and L_{m2} =85 μH and a turns ratio of n_1=n_2=2.5:1. The converter capacitors were DC bus capacitor C_b=560 μF and output capacitor C_o=47 μF. The transformers were designed to be fully demagnetized by the end of each switching cycle and the clamping mechanism was set to clamp the DC bus voltage (the voltage across C_b) at about 120 V.

The components that were used in the prototype are as follows:

- Main MOSFET switch: Fairchild Semiconductor's IRF840
- D_1 – D_4 diodes: Fairchild Semiconductor's RHRP1560
- Bus capacitor C_b: 560 μF, 200 V
- Output capacitor C_o: 47 μF, 65 V
- Voltage transducers: ADJ202N
- Current transducer: LA25-NP
- MOSFET driver: UCC27321P

The proposed control scheme was implemented using a TMS320F28335 DSP microcontroller. The microcontroller's built-in A/D (Analog to Digital) converter was used to get sensed input voltage, output voltage and input current values. Figs. 5.1 and 5.2 show the sensing circuits that were used for the voltages and the input current. These circuits were designed so that all the

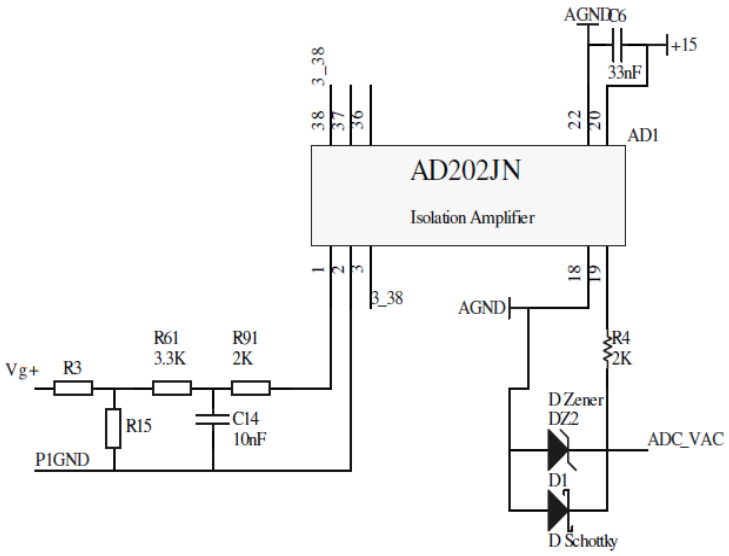


Fig. 5.1 Input voltage and output voltage sensing circuit

voltages and currents were scaled into a range of 0V-3V for the A/D converter. As can be seen in Fig. 5.1, resistors R_3 and R_{15} are voltage division resistors that were used to scale the voltages into the appropriate range for the A/D converter.

Input Current Waveforms and Harmonic Content

Fig. 5.3 and Fig. 5.4 show typical input current waveforms taken at the full output load of 100W. It can be seen that the input current is much more distorted at V_{in} = 230 V than at V_{in} = 100 V. This is because at V_{in} = 230 V, there is more 120 Hz component at the output that needs to be eliminated as more direct power transfer happens due to the DC bus voltage clamping mechanism. Since there is more output voltage ripple that needs to be considered at this voltage, more distortion needs to be introduced into the input current. Fig. 5.5 and 5.6 show the input current harmonic content for V_{in} = 100 V and V_{in} = 230 V. It can be seen that the EN61000-3-2 Class D standard is satisfied, as it should be since the distortion that is introduced in the input current was intentionally pre-set as was designed in Chapter 4.

It should be noted that an operating point of V_{in} = 230 V and full load represents the worst-case operating condition. If the EN61000-3-2 Class D standard can be satisfied under this condition, then it can be satisfied for other operating conditions.

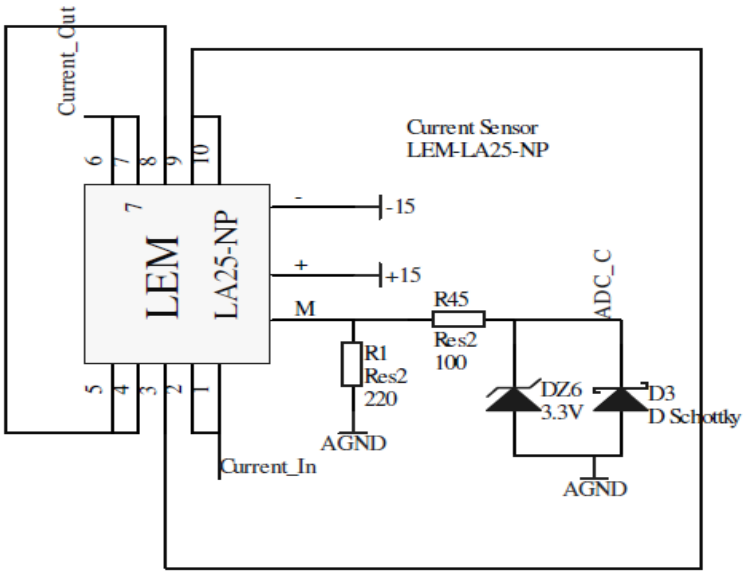


Fig. 5.2 Input current sensing circuit

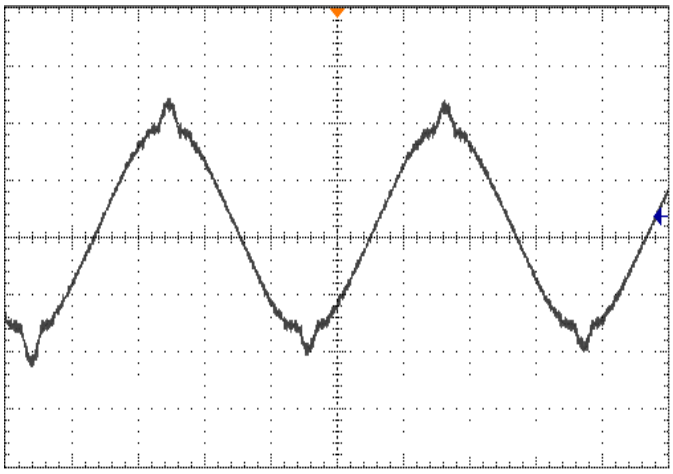


Fig. 5.3 The input current using the proposed control scheme V_{in}=100 V (t: 120μs/div, I: 2A/div)

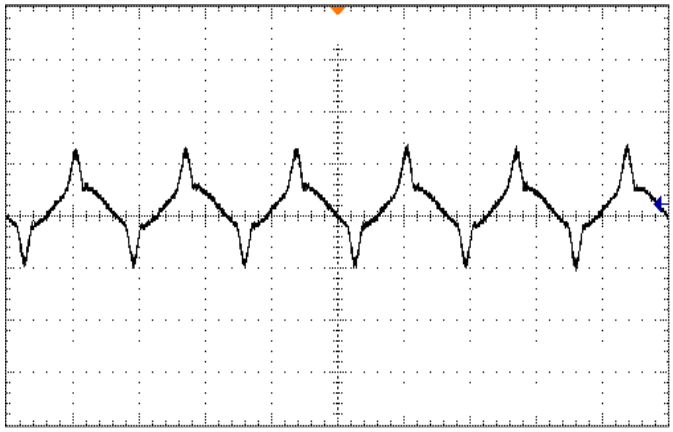


Fig. 5.4 The input current using the proposed control scheme V_{in}=230 V (t: 40μs/div, I: 2A/div)

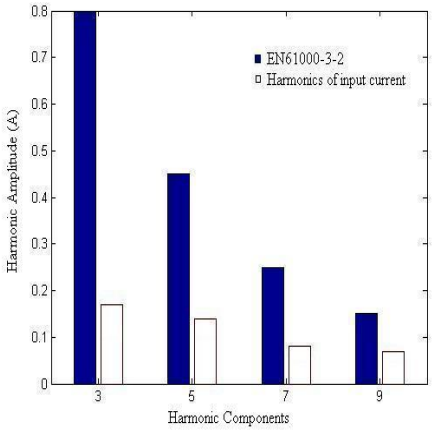


Fig. 5.5 Harmonic content of the input current at V_{in}=100V and EN61000-3-2 limitations

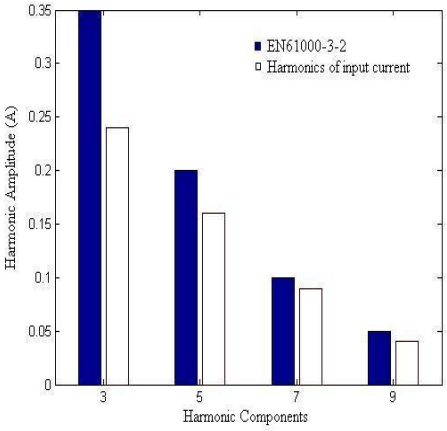


Fig. 5.6 Harmonic content of the input current at Vin=230V and EN61000-3-2 limitations

Output Voltage, Transient Response and Efficiency

Fig. 5.7 shows the output voltage for V_{in} = 230 V over two 60 Hz line cycles (four 120 Hz cycles), with the converter operating with the proposed control scheme. It can be seen that the output voltage ripple in Fig. 5.5 is around 3 V so that the output voltage is about 48 V ± 5%, which is an acceptable tolerance [69]. It should be noted that since more energy is transferred directly to the output when the converter is operating at high input voltage line conditions, the output voltage ripple is at its maximum level under these conditions.

Fig. 5.8 shows how the output voltage reacts when the load is changed from full load to 50%

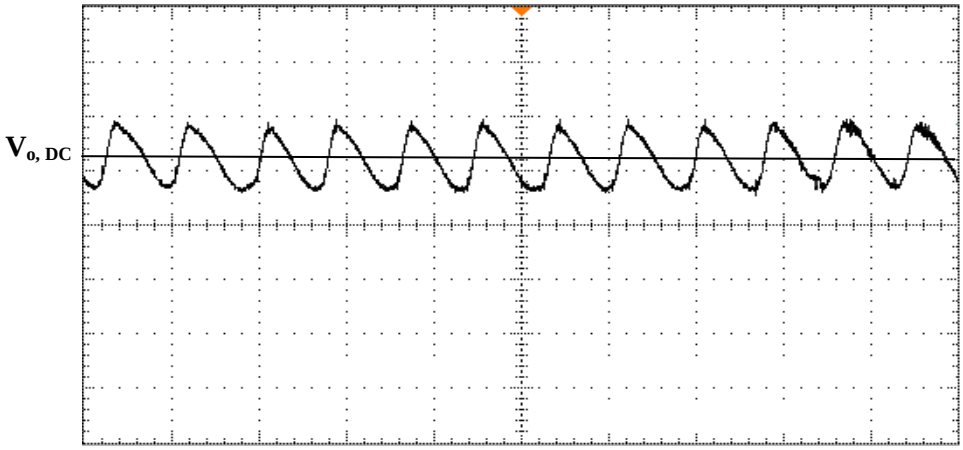


Fig. 5.7 Output voltage of the single-stage PFC converter with the proposed control scheme at V_{in}=230 V (t: 1ms/div, V: 5V/div)

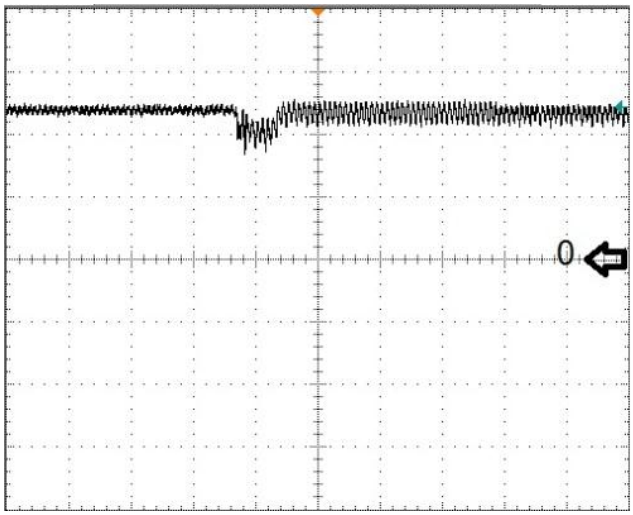


Fig. 5.8 Transient response of the controller with a load change from full load to half load (V_{in}=100V, t: 10ms/div, V: 20V/div)

load. It can be seen that the settling time is around 6 ms, which compares favorably to what has been reported for conventional converters, which is around 350 ms [75],[78].

The DC bus voltage was measured to be about 120 V ± 10% for all line and load conditions. The maximum converter efficiency that was obtained was approximately 80% under high line and full load conditions. This was comparable with other controlled single-stage converters [37], [75]. When it is considered that smaller capacitor sizes were used in the DC bus (due to the clamping mechanism) and the output of this converter (due to the new control scheme) compared to what are typically used in conventional single-stage PFC converters [69], [76], [77], then the SSBBDET converter with the proposed control scheme becomes a very attractive option for AC/DC power conversion.

5.3. Conclusion

Experimental results confirming the feasibility of the SSBBDET converter operating with the proposed control scheme were presented in this chapter. It was shown that the new control scheme allows the converter to operate with tight output regulation and with an acceptable harmonic content as per EN61000-3-2 standards. Moreover, the transient response of the converter was much quicker than what is typically found in single-stage PFC converters implemented with conventional control schemes. The efficiency of the converter compared favorably to that of other previously proposed single-stage PFC converters, especially since it can operate with smaller capacitors in the DC bus and the output compared to what are typically used in conventional single-stage PFC converters,

Chapter 6

Conclusion

6.1. Introduction

In this chapter, the contents and results of the thesis work are summarized, the conclusions that have been reached as a result of this research work are presented, the main contributions of the thesis are expressed and possibilities for future research work are stated.

6.2. Summary

AC/DC power conversion is typically done with two converter stages – an AC/DC front-end converter followed by a DC/DC converter that takes the output of the front-end converter and converts it to the desired output voltage. The front-end AC/DC converter is typically implemented with some sort of power factor correction (PFC) technique to make the input current sinusoidal and in phase with the input voltage. In order to try to reduce the cost of this two-stage AC/DC conversion process, researchers have proposed so-called single-stage converters that can perform AC/DC conversion with just one converter that can simultaneously perform input PFC and DC/DC conversion of an intermediate DC bus voltage.

Single-stage converters are typically implemented with only a single controller to regulate the output voltage. As a result, the intermediate DC bus voltage is unregulated, unlike the intermediate DC bus voltage that is the output of the AC/DC front-end converter of a two-stage converter, which is controlled by the front-end converter. Since this voltage is unregulated, it is dependent on the input line voltage and the output load and thus can vary considerably, which

can create problems in the design of the converter when universal input line (85Vrms-265Vrms) applications are considered. One of these problems is that the converter components must be selected so that they can operate over a wide range of voltages. This is particular true of the DC bus capacitor and the main power transformer. In the case of the DC bus capacitor, sufficient capacitance is needed to filter out high current harmonics in low line applications, yet withstand high voltages in high line applications.

A single-stage converter that was proposed by N. Golbon and G. Moschopoulos in [39], which has been referred to as the Single-Stage Buck-Boost Direct Energy Transfer (SSBBDET) converter in this thesis can operate with a fixed intermediate DC bus voltage, due to a clamping mechanism that can transfer energy away from the DC bus capacitor (so that this capacitor is not overcharged above a preset limit) to the output. This helps reduce the size of the DC bus capacitor as smaller capacitors with lower voltage ratings can be used. The DC bus voltage clamping mechanism, however, increases the output voltage ripple as it superimposes a 120 Hz AC component on top of the output DC voltage, so that output capacitance needs to be increased to filter out this AC component. This is especially true when the converter is operating under high line conditions and the converter is most likely to be in need of the clamping mechanism and transfer energy to the DC bus. The 120 Hz component corresponds to the output voltage and current of the input diode bridge rectifier, which are rectified sinusoidal signals with 120 Hz components.

Increasing the size of the output capacitor to filter the 120 Hz component at the output, however, results in slowing down converter transient response and thus some other means must be used to reduce output voltage ripple. This cannot be done with conventional controllers since an appropriately designed controller must have a low bandwidth voltage loop to prevent the 120 Hz component from distorting the input current; this makes the transient response to be sluggish. If, however, the input current is already distorted, then there is less need to be concerned about output voltage ripple distorting it so that the means that are typically used to keep output voltage ripple from distorting the input current, which slow down transient response, become unnecessary, thus enabling a quicker transient response.

The main objective of this work was to reduce the output voltage ripple of the SSBBDET converter without compromising on transient response. This was done by developing a new

control technique that was based on modifying the conventional average current mode control that is typically used in PFC converters as described in [62]. The main principle behind this technique is that output voltage ripple can be reduced by intentionally distorting the input current as described above. The contents of this thesis can be summarized as follows:

In Chapter 1, basic power electronic concepts that were relevant to this thesis were explained, a literature review of single-stage converters and of commonly used control techniques was performed and the thesis objectives and outline were given.

In Chapter 2, the operation of the SSBBDET converter was discussed. Most of the contents of this chapter were a review of the work presented by N. Golbon and G. Moschopoulos in [39]. In this chapter, the converter's modes of operation were reviewed, an analysis of the converter's steady-state characteristics was presented and several key component values were selected. The main advantage of this converter is that its DC bus voltage variation is significantly less than that of other single-stage PFC converters, which allows smaller size components specially DC bus capacitor to be used. This is the result of buck–boost type input section and clamping of V_C to n_1V_o by the secondary winding of T_1. In this chapter, the operation of the converter and its various modes of operation were explained in detail and key component values were selected by a design procedure. These component values were used in a prototype converter from which experimental results were obtained, as will be shown in Chapter 5 of this thesis.

In Chapter 3, a small-signal state-space model of the SSBBDET converter based on a new averaged state-space model was determined. Conventional approaches fail to accurately model the behaviour of single-stage PFC converters such as the SSBBDET converter because of multiple inductors in their structure (the magnetizing inductances of transformers). A new scheme for the averaged state-space modeling of a single-stage PFC converter with multiple inductors was proposed based on the modification of conventional approach for PWM converters with one inductor. The main idea behind this new scheme is that the general averaged state-space model for PWM converters with one inductor can be applied to each inductor separately and then all these separate models can be merged together to form the averaged state-space model for the SSBBDET converter. A small-signal state-space model and output to duty ratio small-signal transfer functions of the converter was extracted from the new averaged state-space model. This

model and the transfer functions was used later in this thesis to keep the small-signal values at zero so the converter can operate at its pre-defined steady-state condition.

A control strategy for the SSBBDET converter was proposed in Chapter 4. In this chapter, the conventional average current mode control approach for single-stage PFC converters was discussed and it was explained that it results in very slow converter transient response. The proposed control scheme was proposed to address this issue by purposefully distorting the input current reference in the conventional average current mode approach. A mathematical analysis of this technique was performed and the results of this analysis were used to select appropriate parameter values that ensure the proper operation of the SSBBDET converter with the new control scheme. The parameters that were selected were implemented in a prototype converter that was implemented with the proposed control scheme.

Experimental results confirming the feasibility of the SSBBDET converter operating with the proposed control scheme and with the design parameters selected in previous chapters were presented in Chapter 5. It was shown that the new control scheme allowed the converter to operate with tight output regulation and with an acceptable harmonic content as per EN61000-3-2 standards. Moreover, the transient response of the converter was much quicker than what is typically found in single-stage PFC converters implemented with conventional control schemes. The efficiency of the converter was measured and was found to be similar to that of other previously proposed single-stage PFC converters. It should be noted that the SSBBDET converter can operate with smaller capacitors in the DC bus and the output compared to what are typically used in conventional single-stage PFC converters.

6.3. Conclusions

Based on the results provided in Chapter 5, the following conclusions can be made:

1) Distorting the input current in an appropriate manner can result in an excellent output transient response. This is because distorting the input current allows the input current to follow the reference signal more quickly and this leads to faster transient response.
2) The amount of distortion that needs to be added to the input current is not enough to make the input current harmonic content of the SSBBDET converter not comply with EN61000-3-2 class D standards.

3) The worst-case for input current distortion occurs when the SSBBDET converter is operating under high input line and maximum output load power. It is under these circumstances when the amount of energy that is directly transferred from the DC bus to the output through the clamping mechanism that the output voltage ripple is at its peak and thus more input current distortion is needed to reduce it.
4) When designing the controller, the key parameters that need to be considered are k_v and ϕ_L where k_v is the ratio of the DC error of the output voltage over the AC output voltage ripple and ϕ_L is the phase-delay of the controller. These parameters should be designed so that the output voltage ripple is minimized. It was found that values of $k_v = 0.87$ and $\phi_L = -90°$ gave the best results.
5) The maximum converter efficiency was obtained was approximately 80% under high line and full load conditions. This was comparable with other controlled single-stage converters, especially considering the fact that smaller capacitor sizes are used in DC-bus and output of this converter.

6.4. Contributions

The major contributions of this thesis work are as follows:

1) An averaged state-space model of the SSBBDET converter was obtained as well as a small-signal model and the transfer functions of input current and output voltage to the duty cycle were provided. A necessary part of designing a controller for any power electronic converter is to accurately model its behaviour by deriving various models and transfer functions. With this information, an appropriate controller can be designed, whether it is the proposed control scheme or more conventional schemes.
2) The method that was used to determine an average state-space model for a single-stage PFC converter with multiple inductors, like the SSBBDET converter, is novel to the best of the author's knowledge.
3) A new control scheme based on distorting the input current was implemented on the SSBBDET converter. Although the idea of distorting the input current is not in and of itself novel (having been first proposed in [68]) what is novel is the application of the idea to the SSBBDET converter, which is a more sophisticated converter than the front-

end AC-DC boost converter under study in [68]. The basic principle was introduced with favorably comparable performance with other conventional control schemes. The control technique achieves fast transient response and considerable output voltage ripple reduction while the input current is compatible with EN 61000-3-2 class D standards.

4) The feasibility of the proposed control strategy was confirmed using computer simulations and experimental work obtained from a prototype converter.

6.5. Proposal for future work

The following suggestions can be considered for potential future work:

1) The proposed averaged state-space modeling method and the proposed control scheme were only applied on the SSBBDET converter. For future work, it can be applied to other single-stage converters to confirm their superior performance over previously proposed state-space modeling and control methods.
2) For this thesis work, the proposed control strategy was implemented based on average current-mode control. For future work, the proposed control scheme can be implemented with other control schemes such as peak current mode control to see how it performs.

Appendix A

Average Value of the Current Flowing through an Inductor Operating in Discontinuous Conduction Mode (DCM)

In this section, Eq. (3.6), which depicts the average value of the input inductor current of a converter operating in discontinuous conduction mode (DCM) is derived. The current waveform of a DCM operating inductor is shown in Fig. A.1. The following equation can be used to derive the average value of a function over an interval (a, b)

$$\overline{f} = \frac{1}{b-a}\int_a^b f(x)\,dx \tag{A.1}$$

In order to apply this equation to the waveform in Fig. A.1, the waveform should be separated into three separate functions that together form the waveform. These three functions are i_{P1} and i_{P2} that express slopes P_1 and P_2 as indicated in Fig. A.1, and the third function has a zero slope. i_{P1} and i_{P2} can be determined as follows:

$$P_1\colon i_{P1}(t) = \frac{i_{pk}}{d_1 T_s}t \tag{A.2}$$

$$P_2\colon i_{P2}(t) = \frac{-i_{pk}}{d_2 T_s}(t - (d_1 + d_2)T_s) \tag{A.3}$$

Replacing (A.2) and (A.3) into (A.1) gives

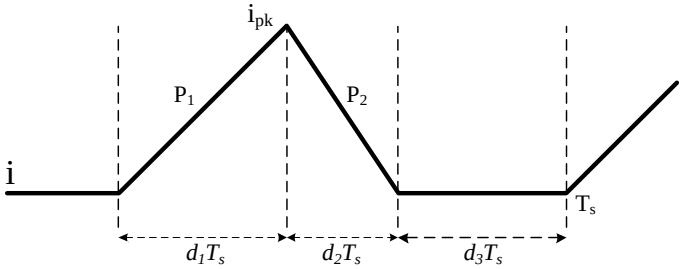


Fig. A.4. Current waveform for an inductor operating in DCM.

$$\bar{i} = \frac{\int_0^{d_1 T_S} i_{P1}(t)dt + \int_{d_1 T_S}^{(d_1+d_2)T_S} i_{P2}(t)dt}{T_S} \tag{A.4}$$

Solving the two integrals (A.4) gives

$$\int_0^{d_1 T_S} i_{P1}(t)\, dt = \int_0^{d_1 T_S} \frac{i_{pk}}{d_1 T_s} t\, dt = \frac{i_{pk}}{2} d_1 T_s \tag{A.5}$$

$$\int_{d_1 T_S}^{(d_1+d_2)T_S} i_{P2}(t)\, dt = \int_{d_1 T_S}^{(d_1+d_2)T_S} \frac{-i_{pk}}{d_2 T_s} (t - (d_1 + d_2)T_s)\, dt$$

$$= \frac{i_{pk}}{2} d_2 T_s \tag{A.6}$$

Substituting (A.5) and (A.6) into (A.4) results in

$$\bar{i} = \frac{\frac{i_{pk}}{2} d_1 T_s + \frac{i_{pk}}{2} d_2 T_s}{T_s} = \frac{i_{pk}}{2}(d_1 + d_2) \tag{A.7}$$

which matches Eq. (3.6) that is used in Chapter 3.

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Curriculum Vitae

Kamran Rezaei, M.E.Sc. Candidate

RESEARCH INTERESTS

- DSP-based Control System Design for Power Converters
- Single-Stage AC/DC Power Electronics Converters
- Digital & Analog Control System Design and Implementation for Power Converters
- Soft-Switching Techniques in Power Converters

EDUCATION

- ***University of Western Ontario (UWO), London, Canada***
  M.E.Sc, Electrical and Computer Engineering (Sept. 2010 to Aug. 2012)
  Thesis Title: A Control Scheme for an AC-DC Single-Stage Buck-Boost PFC Converter with Improved Output Ripple Reduction
  Supervisor: Associate Prof. Gerry Moschopoulos
- ***Sharif University of Technology (SUT), Tehran, Iran***
  B.Sc. in Electrical Engineering, Major: Power (Sept. 2005 – Jul. 2010)
  Thesis Title: *Simulation and Implementation of a nonlinear model predictive control on a PFC-Flyback converter* supervised
  Supervisor: Assistant Prof. Farzad Tahami

HONORS & AWARDS

- Ranked **44th** Among Over 500000 Participants in National University Entrance Exam, Summer 2005
- Awarded *University of Western Ontario Graduate Research Scholarship (WGRS-ECE)*, Sept. 2010 to present
- Awarded *Western Engineering Travel Grant*, Apr. 2012

PUBLICATIONS

- K.Rezaei, G. Moschopoulos "Digital Controller for Sheppard-Taylor Converter Using Optimal Linear Quadratic Regulator" in Canadian Conference on Electrical and Computer Engineering 2012 (CCECE '12), Apr. and May 2012, Montreal, Canada
- F. Tahami, M. R. Abedi, and **K. Rezaei** "*Optimum Nonlinear Model Predictive Controller Design for PFC Flyback Rectifiers*" *in proc.* 2010 IEEE Symposium on Industrial Electronics & Applications (ISIEA 2010), Oct. 2010, Penang, Malaysia.

ACADEMIC EXPERIENCES

- ***University of Western Ontario***
  - **Graduate Research Assistant**, Power Engineering Laboratory, Research on Single-Stage PFCs and Digital Control System Design based on DSP microcontroller for Power Converters, Sept. 2010 to present
  - **Graduate Teaching Assistant**, Faculty of Engineering
    - *ECE3374 Electromechanics*
    - *ECE2241b Electrical Laboratory II*
- ***Sharif University of Technology***
  - **Undergraduate Research Assistant**, Power Electronics Laboratory, Research on DC/DC Power Supplies and Digital Control System Design Using Low-Cost DSP Microcontrollers, Sept. 2009 – Sept. 2010
  - **Teaching Assistant,** Department of Electrical Engineering
    - *Power Systems Analysis*
    - *Power Electronics*
    - *Power Electronics Laboratory*
    - *Electrical Engineering Principles Laboratory*
  - **Laboratory Manual Designer and Coordinator**, Power Electronics Laboratory, Sep. 2009 - Aug 2010

SELECTED PROJECTS

Current Projects

- **M.E.SC. Thesis:** *"A Control Scheme for an AC-DC Single-Stage Buck-Boost PFC Converter with Improved Output Ripple Reduction"* (Sept. 2010 to Aug. 2012)
- "*Small-Signal Analysis and Control Design of Isolated Full-Bridge Boost Converter With Optocoupler Feedback*" (Jul. 2011 to present)

Accomplished Projects

- *"A Comparative Study of Active-Clamped and RCD-Clamped Current-Fed Full-bridge Converters"* (Feb. 2011 - Jul. 2011)
- *"Averaged Modeling and Design of a Digital Controller for a 250W Sheppard-Taylor DC/DC Converter Using State-Feedback with a State-Observer"* (Dec. 2010)
- **B.Sc. Project** : "*Design, Simulation and Implementation of Nonlinear Predictive Control Circuit for PFC-Flyback Rectifiers using low-cost DSP microcontroller"* (Feb. 2010 – Jun. 2010)

OTHER ACADEMIC & PROFESSIONAL ACTIVITIES

- IEEE Student Member, Jan. 2011 to Present
- Research & Development Team Member in Mega-Motor UPS Manufacturing & Importing Company, Spring & Summer 2008
- General Co-Chair of National Conference on *"Restructuring & Deregulation of Power Systems"*, Sharif University of Technology, Fall 2007

RELATED PROFESSIONAL SKILLS

- **Programming Skills:** MATLAB, C++, Assembly
- **Design & Simulation Skills:** SIMPLIS, PowerSIM, Simulink, Orcad Capture/PCB Designer, Pspice, Proteus, Protel DXP PCB Designer
- **Experimental Skills:** EzDsp evaluation boards(F283xx & F28xx)
- **Language Skills:** Farsi(native), English(fluent)

SIGNIFICANT GRADUATE COURSES

- Numerical Analysis of High Frequency Electrical Circuits (**Ranked 1st**)
- High Frequency Power Electronic Converters (**Ranked 1st**)
- Vector Control of Rotating Machines
- Advanced Digital Control Systems
- Design, Modeling & Control of Power Electronics Converters

COMMUNITY & EXTRA-CURRICULAR ACTIVITIES

- Student Council Chair, Electrical Engineering Department, Sharif University of Technology, Sept. 2006 - Sept. 2007
- UWO Alternate Delegate in PSAC National Triennial Conference, Apr. & May 2012
- UWO GTA Needs and Bursaries Evaluation Committee Member, Nov. 2011 - Aug. 2012
- UWO GTA Union Member, Jan. 2011 to Present
- Executive Member of RESANA, Student's extra activities association of ECE department in SUT, Sept. 2005 - Jun. 2010